NOVATEK
聯 詠 科 技

Data Sheet

*for **NT3915***

One-chip Driver IC with internal GRAM
for 262,144 colors 132 RGB x 176 dot TFT LCD

V0.2

INDEX

REVISION HISTORY

NT3915 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	June 2004
0.1	1. Add back light power control feature discription (Page 6) 2. Modify pad dimensions, pad arrangement & pin assignment (Page 8,9) 3. Remove VCIOUT 4. Removed the VREG1OUT VREG2OUT, VgoffH/L, VgoffOUT regulator,for Block Diagram figure. 5. Add VCL and C41P,C41M (Page 12) 6. Modify RESETB1,2,3 to RESETB(Page 14) 7. Modify Table 6 Instruction Table2 for PWM control (Page 28) 8. Add PWM control (Page 58) 9. Add PWM Electrical Characteristics (Page 116)	11/09/2004
0.2	1. Remove VDD3O pin (Page 14) 2. Add dummy pin: TAVPT,TAVNT,TAVIOT (Page 14) 3. Modify pin name: RESETB (Page 124) 4. Modify PWM control item: (1) VFB,FPWM,DPWM (2) Add FSM Control (R3Fh) (3) Modify PWM application circuit 5. Modify application circuit (Page 114)	3/24/2005

FEATURES

132-RGB x 176-dot TFT-LCD display controller/driver IC for 262,144 colors
(396ch-source driver/176ch-gate driver)
18-/16-/9-/8-bit high-speed parallel bus interface (80- and 68- system) and serial peripheral interface (SPI)
High-speed RAM write function (transfer 4-word at a time)
Writing to a window-RAM address area by using a window-address function
Bit-operation function for graphic processing
- – Write-data mask functions in bit units
- – Logical operation in pixel unit and conditional write function

Various color-display control functions
- – 262,144 colors can be displayed at the same time (including gamma adjust)
- – Vertical scroll display function in raster-row units

Internal RAM capacity: 132 x 18 x 176 = 418,176 bits
Low-power operation supports:
- – Power-save mode: standby mode, sleep mode
- – Partial display of two screens in any position
- – Internal charge-pump circuit for generating driving voltage
- – Voltage followers to decrease direct current flow in the LCD drive breeder-resistors
- – Equalizing function for the switching performance of charge-pump circuits and operational amplifiers

Internal oscillation circuit and external hardware reset
Structure for TFT-display retention volume (Cs on COM structure)
Alternating functions for TFT-LCD counter-electrode power
- – Frame / N-line alternating drive of Vcom

Internal power supply circuit
- – Charge-pump circuit: five to nine times, positive-polarity inversion
- – Adjustment of Vcom amplitude: internal 22-level digital potentiometer

DC to DC control circuit for back-light power
Operating voltage
- Apply voltage
  - – VDD to VSS = 2.0 to 2.5 V (non-regulating) (logic voltage range – non-regulated)
  - – VDD3 to VSS = 2.5 to 3.3 V (regulating) (logic voltage range – regulated)
  - – Vci to VSS = 2.5 to 3.3 V (internal reference power-supply voltage)
  - – Vci1 to VSS = 1.7 to 2.75 V (2.5 x 0.68 ~ 2.75) (power supply for charge-pump circuits)
- Generate voltage
  - – For the source driver: AVDD to VSS = 3.5 to 5.5V (power supply for driving circuits)
    GVDD to VSS = 3.3 to 5.3V (reference power supply for grayscale voltages)
  - – For the gate driver: VGH to VGL = 14 to 30 V, VGH to VSS = +7.0 to +16 V,
    Vgoff = (VGL+0.5)V to –7.5V
  - – For the TFT-LCD counter electrode: Vcom amplitude(max) = 6V, VcomH to VSS(max) = GVDD
    VcomL to VSS (max) = 1.0 V to -Vci 1+ 0.5 V

GENERAL DESCRIPTION

The NT3915 is one chip solution for TFT-LCD panel: source driver with built-in memory, gate driver, power IC are integrated on one chip. This IC can display to a maximum of 132-RGB x 176-dot graphics on 260k-color TFT panel.

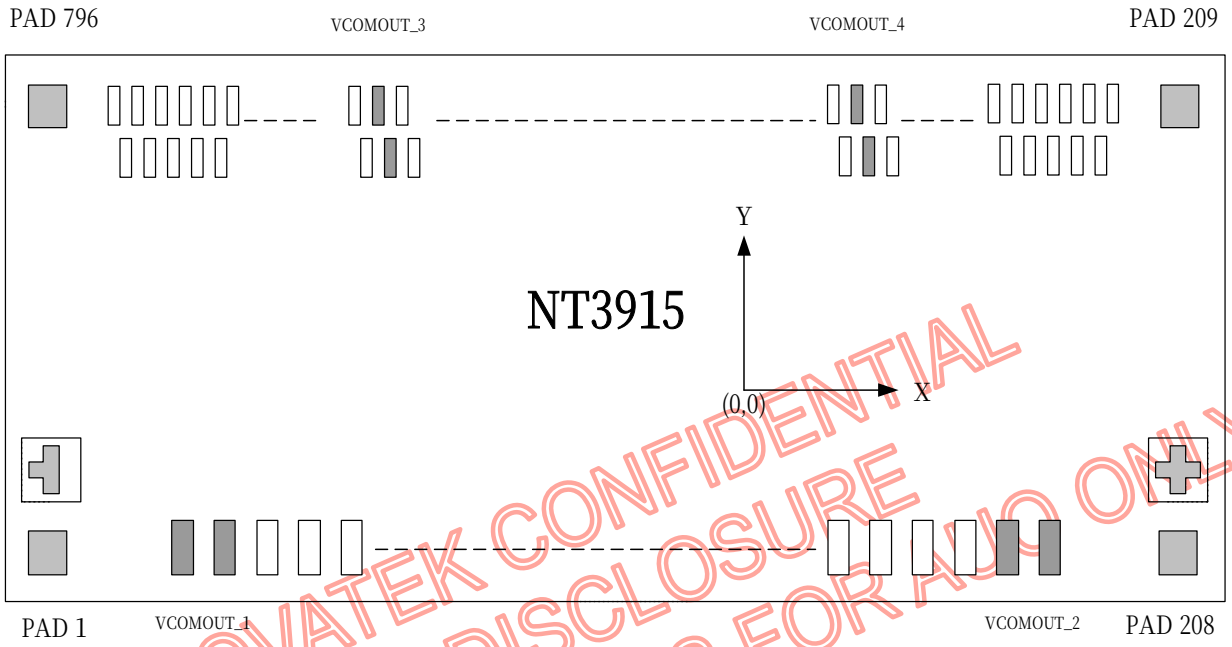
The NT3915 also supports bit-operation functions, 18-/16-/9-/8-bit high-speed bus interface and high-speed RAM-write functions enable efficient data transfer and high-speed rewriting of data to the internal GRAM.

The moving picture area can be specified in internal GRAM by window function. The specified window area can be updated selectively, so that moving picture is able to be displayed simultaneously independent of still picture area.

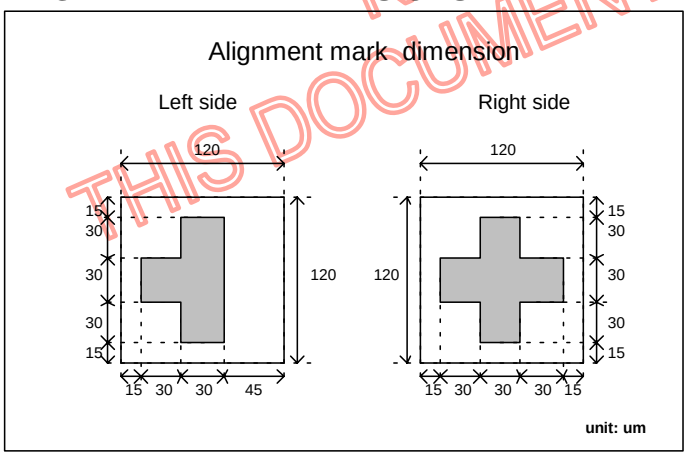
The NT3915 has various functions for reducing the power consumption of a LCD system: operating at low voltage (minimum 1.8V), register-controlled power-save mode, partial display mode and so on. The IC has internal GRAM to store 132-RGB x 176-dot 260k-color image and internal booster that generates the LCD driving voltage, breeder resistance and the voltage follower circuit for LCD driver.

This LSI is suitable for any medium-sized or small portable mobile solution requiring long-term driving capabilities, such as digital cellular phones supporting a web browser, bi-directional pagers, and small PDAs.

PIN ASSIGNMENT (IC face view)



ALIGMENT MARK DIMENSIONS



PAD DIMENSIONS

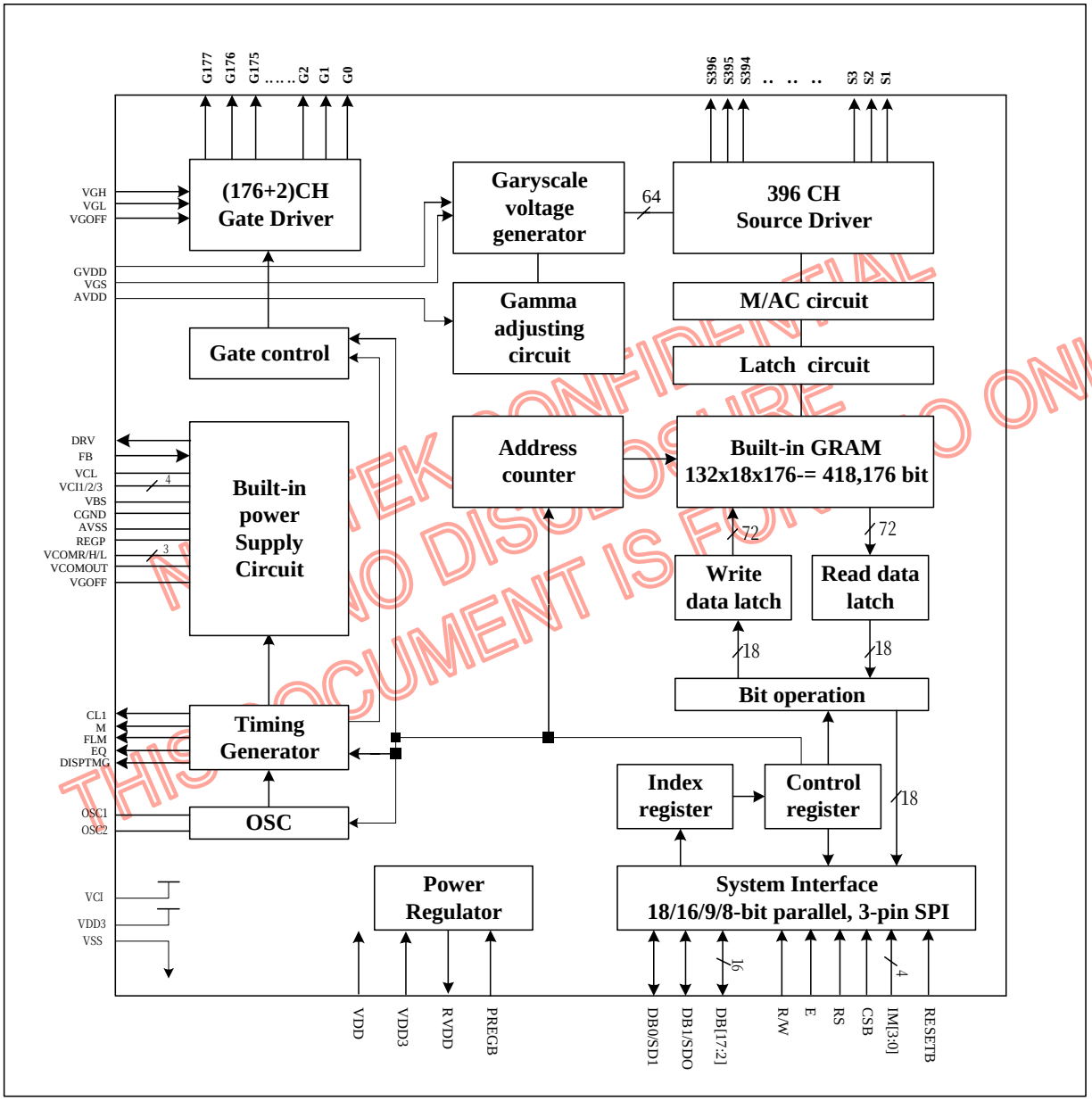
Items	Pad name.	Size		Unit
		X	Y	
Chip size	-	16950	2084	um
Pad dimension	Input Pad	60	97	
	Output Pad	25	88	
	Dummy	60	97	
	Dummy [1], [2],[3],[4]	80	80	
	Dummy [5]	35	97	
	Dummy [6]	50	97	

(Bump Size)

NOTES:

1.Gold bump height (in wafer): 15 ± 3 μm
Gold bump height (in Chip): R ≤ 2 μm (R=Max.-Min.)
2.Scribe line included in this chip size
3.Wafer thickness: 425um

BLOCK DIAGRAM



NT3915 Block Diagram

PIN AND PAD DESCRIPTIONS

POWER SUPPLY PIN

Symbol	I/O	Description
VDD	-	System power supply. As NT3915 has internal regulator, VDD range varies with each mode. Non-regulated mode (PregB = 1) : +2.0 ~ +2.5 V Regulated mode (PregB = 0) : +2.0V
VDD3	-	System power supply for regulator as external power. (VDD3: +2.5 ~ +3.3 V)
AVDD	I/O	A power output pin for source driver block that is generated from power block. Connect a capacitor for stabilization. (AVDD: +3.5 ~ +5.5 V) Connect this pin to VCI2 pin. When not using a charge-pump circuit 1, leave it open.
GVDD	I/O	Standard level for grayscale voltage generator. Connect a capacitor for stabilization.
VCI	-	An internal analog reference power supply. Connect VDD when VDD = 2.5 to 3.3 V. Connect a 2.5 to 3.3V external-voltage power supply when VDD = 2.0 to 2.5 V.
VSS	-	System ground (0V)
CGND	-	System ground level for step up circuit block.
AVSS	-	System ground level for analog circuit block.
VGS	I	Reference voltage for gamma voltage generator.
VCI1	I	A reference voltage in charge-pump circuit 1,4 . Connect a capacitor for stabilization.
VCI2	I	A reference voltage in charge-pump circuit 2.
VCI3	I	A reference voltage in charge-pump circuit 3.
VBS	I	Charge-pump circuit3 control input pin. VGL level is set according to VBS input. When VBS is fixed to “low” level, VGL= -VGH. When VBS is fixed to “high” level, VGL= -VGH+AVDD.
REGP	I/O	Input pins for reference voltages of GVDD when the internal reference-voltage generation circuit is not used. Leave these pins open when the internal reference-voltage generation circuit is used.
VCOMOUT	O	A power supply for the TFT-display counter electrode. The alternating cycle can be set by the M pin. Connect this pin to the TFT-display counter electrode. This pin is also used as equalizing function: When EQ = “High” period, all source driver’s outputs (S1 to S396) are short to Vcom level (Hi-z). In case of VcomL < 0V, equalizing function must not be used. (Set EQ bit (R07h) to be “00” for preventing the abnormal function.)

POWER SUPPLY PIN (CONTINUED)

Symbol	I/O	Description
VcomR	I	A reference voltage of VcomH. When VcomH is externally adjusted, halt the internal adjuster of VcomH by setting the register and insert a variable resistor between GVDD and VSS. When this pin is not externally adjusted, leave it open and adjust VcomH by setting the internal register.
VcomH	O	This pin indicates a high level of Vcom generated in driving the Vcom alternation. Connect this pin to the capacitor for stabilization.
VcomL	O	When the Vcom alternation is driven, this pin indicates a low level of Vcom. An internal register can be used to adjust the voltage. Connect this pin to a capacitor for stabilization. When the VCOMG bit is low, the VcomL output stops and a capacitor for stabilization is not needed.
VGH	O	A positive power output pin for gate driver, internal charge-pump circuits, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. Connect this pin to VCI3 pin. When not using a charge-pump circuit 2, leave it open.
VGL	O	A Negative power output pin for gate driver, bias circuits, and operational amplifiers. Connect a capacitor for stabilization. When internal VGL generator is not used, connect an external-voltage power supply higher than –16 V.
Vgoff	I	Power supply pin for off level for gate of TFT.
VCL	I/O	A power supply pin for generating VcomL.
C11P,C11M ~ C23P,C23M	-	Connect the charge-pump capacitor according to the step-up factor.
C31P, C31M	-	Connect a charge-pump capacitor for generating the VGL level.
C41P,C41M	-	Connect a charge-pump capacitor for generating the VCL level.

SYSTEM INTERFACE PIN

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>IM3-1,
IM0/ID</td><td>I</td><td>Selects the MPU interface mode:
<table>
<tr><th>IM3</th><th>IM2</th><th>IM1</th><th>IM0/ID</th><th>MPU interface mode</th><th>DB PIN assign</th></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 16-bit bus interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 8bit bus interface</td><td>DB17-10</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 16bit bus interface</td><td>DB17-10, DB8-1</td></tr>
<tr><td>VSS</td><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 8bit bus interface</td><td>DB17-10</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VSS</td><td>ID</td><td>Serial peripheral interface (SPI)</td><td>DB1-0</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>VDD3</td><td>*</td><td>Non-selecting</td><td>-</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VSS</td><td>VSS</td><td>68-system 18-bit bus interface</td><td>DB17-0</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VSS</td><td>VDD3</td><td>68-system 9bit bus interface</td><td>DB17-9</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VDD3</td><td>VSS</td><td>80-system 18bit bus interface</td><td>DB17-0</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>VDD3</td><td>VDD3</td><td>80-system 9bit bus interface</td><td>DB17-9</td></tr>
<tr><td>VDD3</td><td>VDD3</td><td>*</td><td>*</td><td>Non-selecting</td><td>-</td></tr>
</table>
When a SPI mode is selected, the IM0 pin is used as ID setting bit for a device code.</td></tr>
<tr><td>CSB</td><td>I</td><td>Chip select signal input pin.
Low: NT3915 is selected and can be accessed
High: NT3915 is not selected and cannot be accessed
Must be fixed at VSS level when not used.</td></tr>
<tr><td>RS</td><td>I</td><td>Register select pin.
Low: Index/status, High: Control</td></tr>
<tr><td>E
(/WR,SCL)</td><td>I</td><td>
<table>
<tr><th>IM2</th><th>IM1</th><th>Pin func.</th><th>MPU type</th><th>Pin description</th></tr>
<tr><td>VSS</td><td>VSS</td><td>E</td><td>68-system</td><td>Read/Write operation enable pin.</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>/WR</td><td>80-system</td><td>Write strobe signal input pin.
Data is fetched at the low level.</td></tr>
<tr><td>VDD3</td><td>VSS</td><td>SCL</td><td>serial peripheral interface (SPI)</td><td>the synchronous clock signal input pin</td></tr>
</table>
</td></tr>
<tr><td>R/W
(/RD)</td><td>I</td><td>
<table>
<tr><th>IM2</th><th>IM1</th><th>Pin func.</th><th>MPU type</th><th>Pin description</th></tr>
<tr><td>VSS</td><td>VSS</td><td>R/W</td><td>68-system</td><td>Read/Write operation selection pin.
Low: Write , High: Read</td></tr>
<tr><td>VSS</td><td>VDD3</td><td>/RD</td><td>80-system</td><td>Read strobe signal input pin.
Read out data at the low level.</td></tr>
</table>
When SPI mode is selected, fix this pin at VSS level.</td></tr>
<tr><td>DB0/SDI</td><td>I/O</td><td>Bi-directional data bus.
18-bit interface : DB 17-0
16-bit interface : DB 17-10, DB 8-1
9-bit interface : DB 17-9
8-bit interface : DB 17-10
Fix DB0 to the VDD3 or VSS level if the pin is not in use.
For a serial peripheral interface (SPI), input data is fetched at the rising edge of the SCL signal.</td></tr>
</table>

SYSTEM INTERFACE PIN(CONTINUED)

Symbol	I/O	Description
DB1/SDO	I/O	Bi-directional data bus. 18-bit interface : DB 17-0 16-bit interface : DB 17-10, DB 8-1 9-bit interface : DB 17-9 8-bit interface : DB 17-10 Fix DB1 to the VDD3 or VSS level if the pin is not in use. For a serial peripheral interface (SPI), serves as the serial data output pin (SDO). Successive bits are output at the falling edge of the SCL signal.
DB17-DB2	I/O	Bi-directional data bus. 18-bit interface : DB 17-0 16-bit interface : DB 17-10, DB 8-1 9-bit interface : DB 17-9 8-bit interface : DB 17-10 Fix unused pin to the VDD3 or VSS level.
RESETB	I	Reset pin. Initializes the LSI when low. Must be reset after power-on.

BACK LIGHT CONTROL PIN

Symbol	I/O	Description
FB	I	Main boost regulator feedback input. Connect feedback resistive divider to GND. FB threshold is 0.6 V nominal.
DRV	O	Power transistor gate signal for the boost converter.

DUMMY PIN

Symbol	I/O	Description
VSSO	-	Output dummy pin for mode setting. Connect these pin to adjacent logic input pin. Must be left open when not used.
Dummy[1]~[6]	-	Dummy pin. No connected.
TESTB0~2	-	Test pin. No connected.
TESTC0~2	-	Test pin. No connected.
TESTR0~2	-	Test pin. No connected.
TEST1~2	-	Test pin. No connected.
TESTV1~2	-	Test pin. No connected.
MTEST1~2	-	Test pin. No connected.
TEST	-	Test pin. No connected.
TS6~7	-	Test pin. No connected.
DCTEST	-	Test pin. No connected.
TESTA2~4	-	Test pin. No connected.
VTESTS	-	Test pin. No connected.
TAVPT	-	Test pin. No connected.
TAVNT	-	Test pin. No connected.
TAVIOT	-	Test pin. No connected.

DISPLAY PIN

Symbol	I/O	Description
S1 - S396	O	Source driver output pins. The SS bit can change the shift direction of the source signal. For example, if SS = 0, gray data of S1 is read from RAM address 0000h. If SS = 1, contents of is RAM address 0000h is out from S396. S1, S4, S7, ... S(3n-1) : display Red (R) (SS = 0) S2, S5, S8, ... S(3n-2) : display Green (G) (SS = 0) S3, S6, S9, ... S(3n) : display Blue (B) (SS = 0)
G1 - G176	O	Gate driver output pins. The output of driving circuit is whether VGH or Vgoff. VGH : gate-ON level Vgoff : gate-OFF level
G0, G177	O	Gate driver output pins for IC maker's testing. Please leave it disconnected.
CL1	O	Output pin for raster-row clock pulse.
M	O	Output pin for AC-cycle signal.
FLM	O	Output pin for frame-start pulse.
EQ	O	Output pin for timing for equalizing. Low : Normal display, High : Equalizing
DISPTMG	O	Output pin for Gate off signal. High : Normal output Low : Non-display

MISCELLANEOUS CONTROL PIN

Symbol	I/O	Description
OSC1/ OSC2	I/O	Connect an external resistor for R-C oscillation. When input the clock from outside, input to OSC1, and open OSC2.
PREGB	I	Internal power regulator control input pin. When the internal regulated power(RVDD) is used as VDD, PREGB is fixed to "low" level. When the external logic power (VDD3) is used as VDD, PREGB is fixed to "high" level.
RVDD	O	Internal power regulated-VDD output (typ. 2.0V). When PREGB is "low", RVDD is connected to VDD pin. When PREGB is "high", leave this pin open.

FUNCTION DESCRIPTION

SYSTEM INTERFACE

The NT3915 has five high-speed system interfaces: an 80-system 18-/16-/9-/8-bit bus, a 68-system 18-/16-/9-/8-bit bus, and a serial interface (SPI: Serial Peripheral Interface). The IM3-0 pins select the interface mode.

The NT3915 has three 18-bit registers: an index register (IR), a write data register (WDR), and a read data register (RDR). The IR stores index information for control register and GRAM. The WDR temporarily stores data to be written into control register and GRAM. The RDR temporarily stores data read from GRAM. Data written into the GRAM from MPU is initially written to the WDR and then written to the GRAM automatically. Data is read through the RDR when reading from the GRAM, and the first read data is invalid and the second and the following data are valid. When a logic operation is performed inside of the NT3915 by using the display data stored in the GRAM and the data written from the MPU, the data read through the RDR is used. Accordingly, the MPU does not need to read data twice or to fetch the read data into the MPU. This enables high-speed processing.

Execution time for instruction, except oscillation start, is 0-clock cycle so that instructions can be written in succession.

SYSTEM	R/W /RD	E /WR	RS	Operations
68	0	1	0	Write index to IR
	1	1	0	Read internal status
	0	1	1	Write to control register and GRAM through WDR
	1	1	1	Read from GRAM through RDR
80	1	0	0	Write index to IR
	0	1	0	Read internal status
	1	0	1	Write to control register and GRAM through WDR
	0	1	1	Read from GRAM through RDR

Table 1. Register Selection (18-/16-/9-/8- Parallel Interface)

R/W bit	RS bit	Operation
0	0	Write index to IR
1	0	Read internal status
0	1	Write data to control register and GRAM through WDR
1	1	Read data from GRAM through RDR

Table 2. Register Selection (Serial Peripheral Interface)

BIT OPERATION

The NT3915 supports the following functions: a write data mask function that selects and writes data to GRAM in bit unit, a logic operation function that performs logic operations or conditional determination on the display data set in GRAM and writes to GRAM. These functions can greatly reduce the processing loads of the MPU graphics software and can rewrite the display data in the GRAM at high speed. For details, see the Graphics Operation Function section.

ADDRESS COUNTER (AC)

The address counter (AC) assign address to GRAM. When an address-set-instruction is written to the IR, the address information is sent from IR to AC. After writing to the GRAM, the address value of AC is automatically increased/decreased by 1 according to ID1-0 bit of control register. After reading data from GRAM, the AC is not updated. A window address function allows data to be written only to a window area specified by GRAM.

GRAPHICS RAM (GRAM)

The graphics RAM (GRAM) has 18-bits/pixel and stores the bit-pattern data for 132-RGB x 176-dot display.

GRAYSCALE VOLTAGE GENERATOR

The grayscale voltage circuit generates a certain voltage level that is specified by the grayscale ϒ-adjusting resistor for LCD driver circuit. By use of the generator, 262,144 colors can be displayed at the same time. For details, see the ϒ-adjusting resistor section.

TIMING GENERATOR

The timing generator generates timing signals for the operation of internal circuits such as GRAM. The GRAM read timing for display and the internal operation timing for MPU access is generated separately to avoid interference with one another. Several important timing signals can be monitored via signal monitoring pin (M, FLM, CL1, EQ, DISPTMG).

OSCILLATION CIRCUIT (OSC)

The NT3915 can provide R-C oscillation simply through the addition of an external oscillation-resistor between the OSC1 and OSC2 pin. The appropriate oscillation frequency for operating voltage, display size, and frame frequency can be obtained by adjusting the external-resistor value. Clock pulse can also be supplied externally. Since R-C oscillation stops during the standby mode, current consumption can be reduced. For details, see the Oscillation Circuit section.

SOURCE DRIVER CIRCUIT

The liquid crystal display source driver circuit consists of 396 drivers (S1 to S396).
Display pattern data is latched when 396-bit data has arrived. The latched data then enables the source drivers to generate drive waveform outputs. The SS bit can change the shift direction of 396-bit data by selecting an appropriate direction for the device-mounted configuration.

GATE DRIVER CIRCUIT

The liquid crystal display gate driver circuit consists of 178 gate drivers (G0 to G177).
The VGH or Vgoff level is output by the signal from the gate control circuit. G0 and G177 are IC maker's test pins.

SYSTEM INTERFACE AND GRAM ADDRESS SETTING

GRAM ADDRESS SETTING (SS="0")

When SS bit is 0 (source output shift direction: right) and BGR bit is 0 (RGB sequence: right) that can be set in R01h register, GRAM address is set as follows:

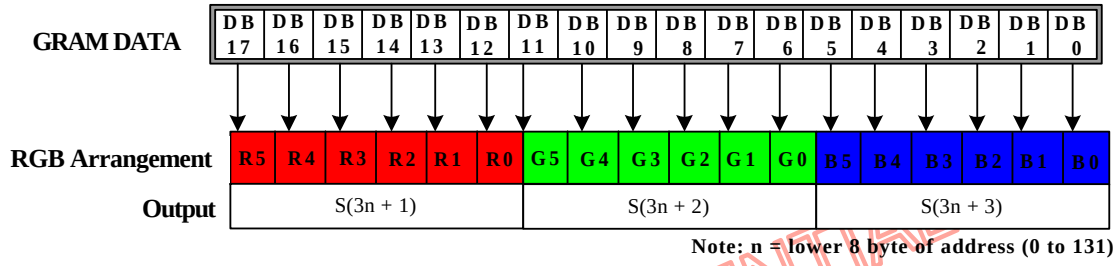
S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0			.....	DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0		
G1	G176	"0000"H			"0001"H			"0002"H			"0003"H			.....	"0080"H			"0081"H			"0082"H			"0083"H		
G2	G175	"0100"H			"0101"H			"0102"H			"0103"H			.....	"0180"H			"0181"H			"0182"H			"0183"H		
G3	G174	"0200"H			"0201"H			"0202"H			"0203"H			.....	"0280"H			"0281"H			"0282"H			"0283"H		
G4	G173	"0300"H			"0301"H			"0302"H			"0303"H			.....	"0380"H			"0381"H			"0382"H			"0383"H		
G5	G172	"0400"H			"0401"H			"0402"H			"0403"H			.....	"0480"H			"0481"H			"0482"H			"0483"H		
G6	G171	"0500"H			"0501"H			"0502"H			"0503"H			.....	"0580"H			"0581"H			"0582"H			"0583"H		
G7	G170	"0600"H			"0601"H			"0602"H			"0603"H			.....	"0680"H			"0681"H			"0682"H			"0683"H		
G8	G169	"0700"H			"0701"H			"0702"H			"0703"H			.....	"0780"H			"0781"H			"0782"H			"0783"H		
G9	G168	"0800"H			"0801"H			"0802"H			"0803"H			.....	"0880"H			"0881"H			"0882"H			"0883"H		
G10	G167	"0900"H			"0901"H			"0902"H			"0903"H			.....	"0980"H			"0981"H			"0982"H			"0983"H		
G11	G166	"0A00"H			"0A01"H			"0A02"H			"0A03"H			.....	"0A80"H			"0A81"H			"0A82"H			"0A83"H		
G12	G165	"0B00"H			"0B01"H			"0B02"H			"0B03"H			.....	"0B80"H			"0B81"H			"0B82"H			"0B83"H		
G13	G164	"0C00"H			"0C01"H			"0C02"H			"0C03"H			.....	"0C80"H			"0C81"H			"0C82"H			"0C83"H		
G14	G163	"0D00"H			"0D01"H			"0D02"H			"0D03"H			.....	"0D80"H			"0D81"H			"0D82"H			"0D83"H		
G15	G162	"0E00"H			"0E01"H			"0E02"H			"0E03"H			.....	"0E80"H			"0E81"H			"0E82"H			"0E83"H		
G16	G161	"0F00"H			"0F01"H			"0F02"H			"0F03"H			.....	"0F80"H			"0F81"H			"0F82"H			"0F83"H		
G17	G160	"1000"H			"1001"H			"1002"H			"1003"H			.....	"1080"H			"1081"H			"1082"H			"1083"H		
G18	G159	"1100"H			"1101"H			"1102"H			"1103"H			.....	"1180"H			"1181"H			"1182"H			"1183"H		
G19	G158	"1200"H			"1201"H			"1202"H			"1203"H			.....	"1280"H			"1281"H			"1282"H			"1283"H		
G20	G157	"1300"H			"1301"H			"1302"H			"1303"H			.....	"1380"H			"1381"H			"1382"H			"1383"H		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G169	G8	"A800"H			"A801"H			"A802"H			"A803"H			.....	"A880"H			"A881"H			"A882"H			"A883"H		
G170	G7	"A900"H			"A901"H			"A902"H			"A903"H			.....	"A980"H			"A981"H			"A982"H			"A983"H		
G171	G6	"AA00"H			"AA01"H			"AA02"H			"AA03"H			.....	"AA80"H			"AA81"H			"AA82"H			"AA83"H		
G172	G5	"AB00"H			"AB01"H			"AB02"H			"AB03"H			.....	"AB80"H			"AB81"H			"AB82"H			"AB83"H		
G173	G4	"AC00"H			"AC01"H			"AC02"H			"AC03"H			.....	"AC80"H			"AC81"H			"AC82"H			"AC83"H		
G174	G3	"AD00"H			"AD01"H			"AD02"H			"AD03"H			.....	"AD80"H			"AD81"H			"AD82"H			"AD83"H		
G175	G2	"AE00"H			"AE01"H			"AE02"H			"AE03"H			.....	"AE80"H			"AE81"H			"AE82"H			"AE83"H		
G176	G1	"AF00"H			"AF01"H			"AF02"H			"AF03"H			.....	"AF80"H			"AF81"H			"AF82"H			"AF83"H		

Table 3. GRAM address (SS="0")

Data fetch from GRAM for display when SS=0 is shown in the following figure.

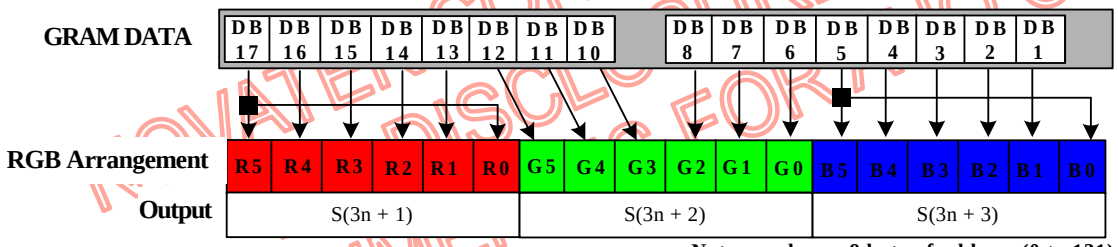
SYSTEM INTERFACE

18-bit System interface



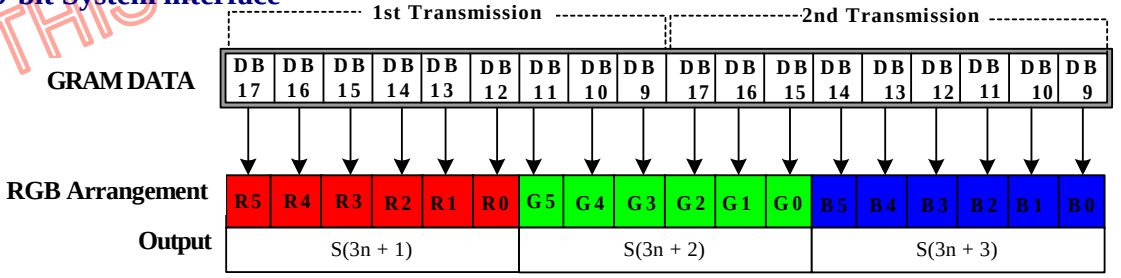
Note: n = lower 8 byte of address (0 to 131)

16-bit System interface



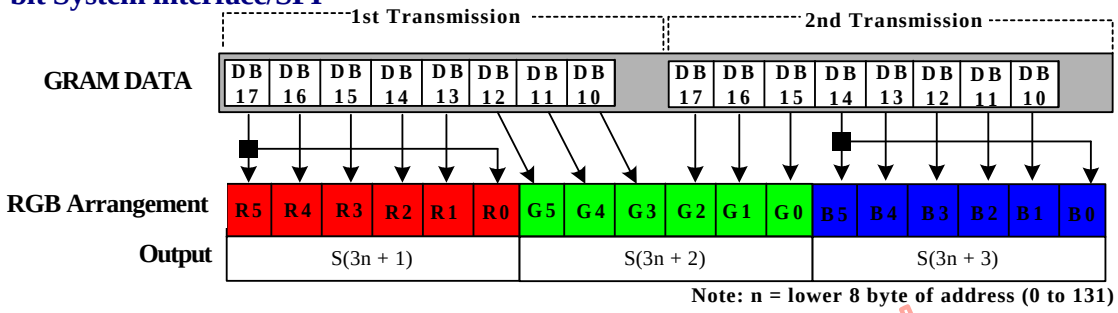
Note: n = lower 8 byte of address (0 to 131)

9-bit System interface



Note: n = lower 8 byte of address (0 to 131)

8-bit System interface/SPI



Note: n = lower 8 byte of address (0 to 131)

GRAM ADDRESS SETTING (SS="1")

When SS bit is 1 (source output shift direction: reversed) and BGR bit is 1 (RGB sequence: reversed) that can be set in R01h register, GRAM address is set as follows:

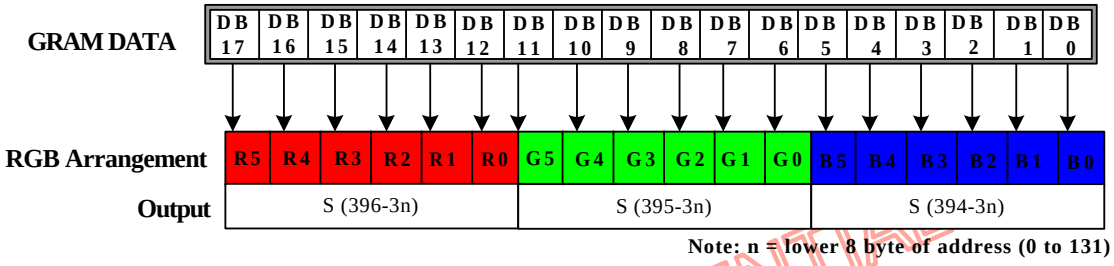
S/G Output		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	.....	S385	S386	S387	S388	S389	S390	S391	S392	S393	S394	S395	S396
GS=0	GS=1	DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0			.....	DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0			DB.....DB 17 0		
G1	G176	"0083"H			"0082"H			"0081"H			"0080"H			.....	"0003"H			"0002"H			"0001"H			"0000"H		
G2	G175	"0183"H			"0182"H			"0181"H			"0180"H			.....	"0103"H			"0102"H			"0101"H			"0100"H		
G3	G174	"0283"H			"0282"H			"0281"H			"0280"H			.....	"0203"H			"0202"H			"0201"H			"0200"H		
G4	G173	"0383"H			"0382"H			"0381"H			"0380"H			.....	"0303"H			"0302"H			"0301"H			"0300"H		
G5	G172	"0483"H			"0482"H			"0481"H			"0480"H			.....	"0403"H			"0402"H			"0401"H			"0400"H		
G6	G171	"0583"H			"0582"H			"0581"H			"0580"H			.....	"0503"H			"0502"H			"0501"H			"0500"H		
G7	G170	"0683"H			"0682"H			"0681"H			"0680"H			.....	"0603"H			"0602"H			"0601"H			"0600"H		
G8	G169	"0783"H			"0782"H			"0781"H			"0780"H			.....	"0703"H			"0702"H			"0701"H			"0700"H		
G9	G168	"0883"H			"0882"H			"0881"H			"0880"H			.....	"0803"H			"0802"H			"0801"H			"0800"H		
G10	G167	"0983"H			"0982"H			"0981"H			"0980"H			.....	"0903"H			"0902"H			"0901"H			"0900"H		
G11	G166	"0A83"H			"0A82"H			"0A81"H			"0A80"H			.....	"0A03"H			"0A02"H			"0A01"H			"0A00"H		
G12	G165	"0B83"H			"0B82"H			"0B81"H			"0B80"H			.....	"0B03"H			"0B02"H			"0B01"H			"0B00"H		
G13	G164	"0C83"H			"0C82"H			"0C81"H			"0C80"H			.....	"0C03"H			"0C02"H			"0C01"H			"0C00"H		
G14	G163	"0D83"H			"0D82"H			"0D81"H			"0D80"H			.....	"0D03"H			"0D02"H			"0D01"H			"0D00"H		
G15	G162	"0E83"H			"0E82"H			"0E81"H			"0E80"H			.....	"0E03"H			"0E02"H			"0E01"H			"0E00"H		
G16	G161	"0F83"H			"0F82"H			"0F81"H			"0F80"H			.....	"0F03"H			"0F02"H			"0F01"H			"0F00"H		
G17	G160	"1083"H			"1082"H			"1081"H			"1080"H			.....	"1003"H			"1002"H			"1001"H			"1000"H		
G18	G159	"1183"H			"1182"H			"1181"H			"1180"H			.....	"1103"H			"1102"H			"1101"H			"1100"H		
G19	G158	"1283"H			"1282"H			"1281"H			"1280"H			.....	"1203"H			"1202"H			"1201"H			"1200"H		
G20	G157	"1383"H			"1382"H			"1381"H			"1380"H			.....	"1303"H			"1302"H			"1301"H			"1300"H		
⋮	⋮	⋮			⋮			⋮			⋮			⋮	⋮			⋮			⋮			⋮		
G169	G8	"A883"H			"A882"H			"A881"H			"A880"H			.....	"A803"H			"A802"H			"A801"H			"A800"H		
G170	G7	"A983"H			"A982"H			"A981"H			"A980"H			.....	"A903"H			"A902"H			"A901"H			"A900"H		
G171	G6	"AA83"H			"AA82"H			"AA81"H			"AA80"H			.....	"AA03"H			"AA02"H			"AA01"H			"AA00"H		
G172	G5	"AB83"H			"AB82"H			"AB81"H			"AB80"H			.....	"AB03"H			"AB02"H			"AB01"H			"AB00"H		
G173	G4	"AC83"H			"AC82"H			"AC81"H			"AC80"H			.....	"AC03"H			"AC02"H			"AC01"H			"AC00"H		
G174	G3	"AD83"H			"AD82"H			"AD81"H			"AD80"H			.....	"AD03"H			"AD02"H			"AD01"H			"AD00"H		
G175	G2	"AE83"H			"AE82"H			"AE81"H			"AE80"H			.....	"AE03"H			"AE02"H			"AE01"H			"AE00"H		
G176	G1	"AF83"H			"AF82"H			"AF81"H			"AF80"H			.....	"AF03"H			"AF02"H			"AF01"H			"AF00"H		

Table 4. GRAM address (SS="1")

Data fetch from GRAM for display when SS=1 is shown in the following figure.

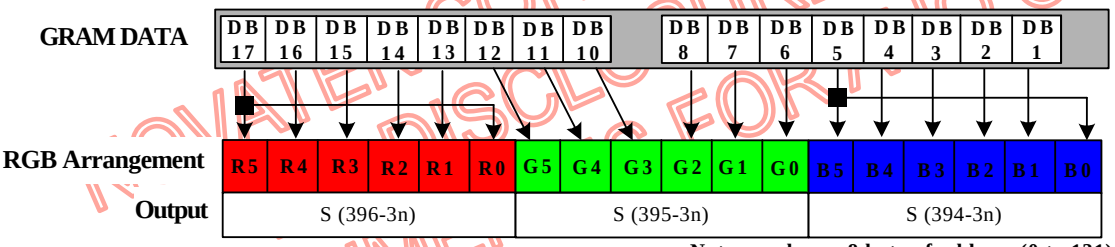
SYSTEM INTERFACE

18-bit System interface



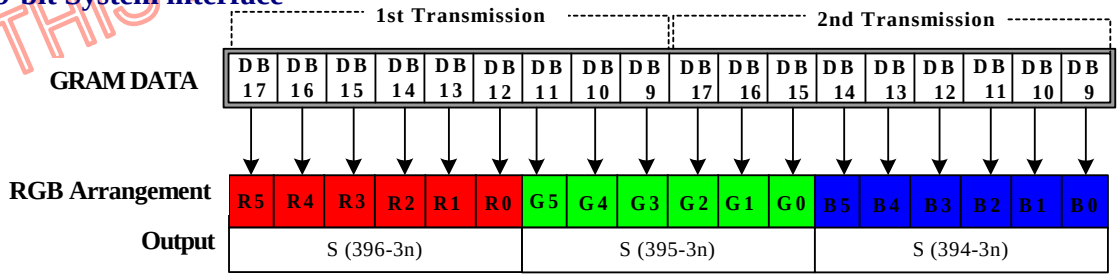
Note: n = lower 8 byte of address (0 to 131)

16-bit System interface



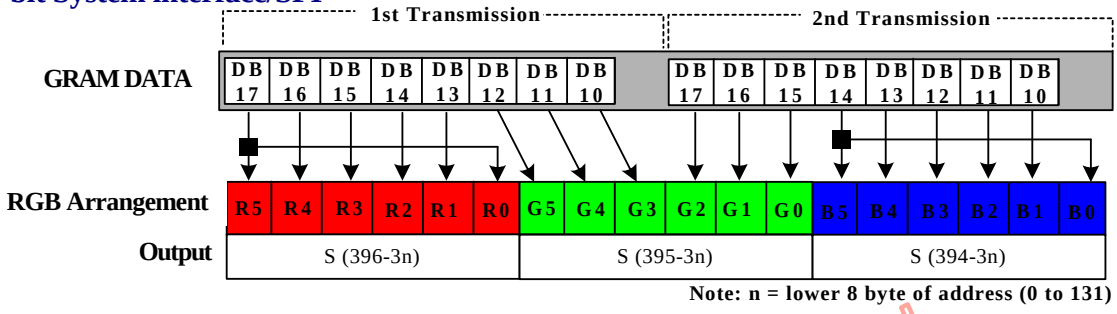
Note: n = lower 8 byte of address (0 to 131)

9-bit System interface



Note: n = lower 8 byte of address (0 to 131)

8-bit System interface/SPI



Note: n = lower 8 byte of address (0 to 131)

INSTRUCTIONS

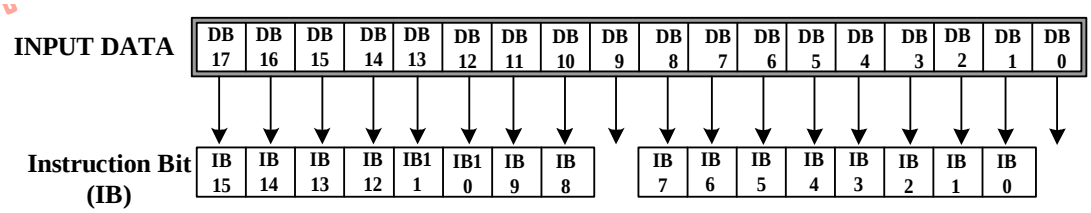
The NT3915 uses the 18-bit bus architecture. Before the internal operation of the NT3915 starts, control information is temporarily stored in the registers described below to allow high-speed interfacing with a high performance microcomputer. The internal operation of the NT3915 is determined by signals sent from the microcomputer. These signals, which include the register selection signal (RS), the read/write signal (R/W), and the data bus signals (DB17 to DB0), make up the NT3915 instructions.
There are nine categories of instructions that:

- Specify the index
- Read the status
- Control the display
- Control power management
- Process the graphics data
- Set internal GRAM addresses
- Transfer data to and from the internal GRAM
- Set grayscale level for the internal grayscale palette table
- Interface with the gate driver and power supply IC

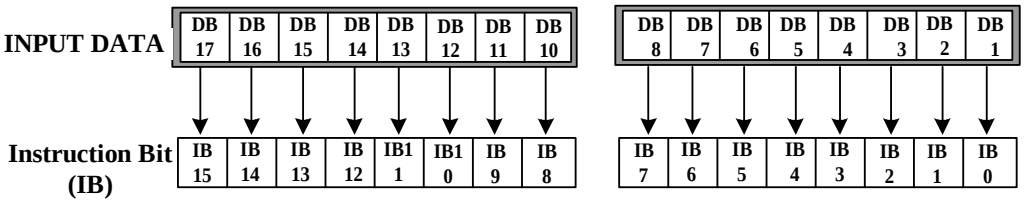
Normally, instructions that write data are used the most. However, an auto-update of internal GRAM addresses after each data write can lighten the microcomputer program load. As instructions are executed in 0 cycles, they can be written in succession.

The 16-bit instruction assignment differ from interface-setup (18-/16-/9-/8-/SPI), so instructions should be fetched according to the data format shown below:

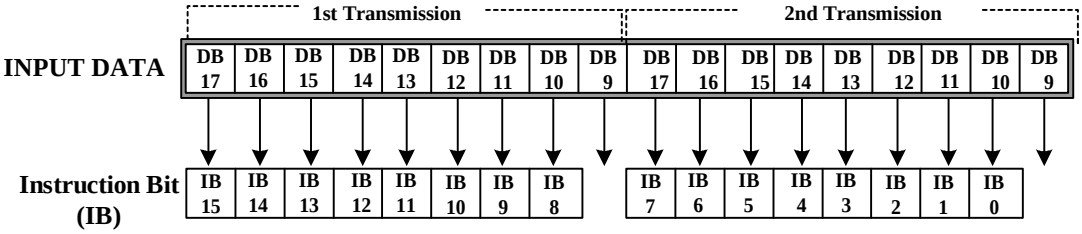
18-bit System interface



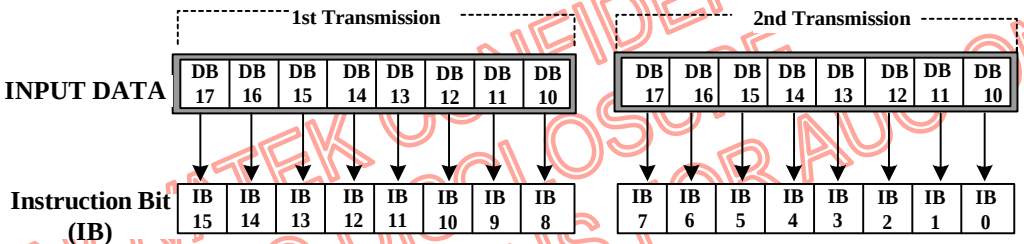
16-bit Interface



9-bit Interface(2-Transfer per pixel)



8-bit Interface/SPI (2-Transfer per pixel)



INSTRUCTION TABLE

Reg. No	R /W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
IR	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0	**Index /** Sets the index register value
SR	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0	**Status read /** Reads the internal status of the NT3915
R00h	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1	**Start oscillation (R00H) /** Starts the oscillation circuit
	1	1	0	0	1	1	1	0	0	1	0	0	0	1	0	0	0	1	**Device code read /** Read 3911
R01h	0	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0	**Driver output control(R01H) /** SM: gate driver division drive control GS: gate driver shift direction SS: source driver shift direction NL4-0: number of driving lines
R02h	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0	**LCD-Driving-waveform control (R02H)/** FLD1-0: number of interlaced field B/C: LCD drive AC waveform EOR: Exclusive OR-ing the AC waveform NW5-0: number of n-raster-row of C-pattern
R03h	0	1	0	0	0	0	0	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB	**Power Control (1) (R03H) /** BT2-0: DC1-0: AP2-0: SLP: STB: s
R05h	0	1	0	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0	**Entry mode(R05H) /** BGR: RGB swap control HWM: high-speed RAM write I/D1-0: address counter Increment / Decrement control AM: horizontal / vertical RAM update LG2-0: Logic operation control
R06h	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0	**Compare register (R06H)/** CP15-0: compare register setting
R07h	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0	**Display control (R07H) /** PT1-0: Non-display area source output control VLE2-1: 1st/2nd partial vertical scroll SPT: 1st/2nd partial display enable GON: gate-off to be VSS level DTE:DISPTMG to be VSS level CL: 8-color display mode enable REV: display area inversion drive D1-0: source output control
R0Bh	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0	**Frame cycle control (R0BH)/** NO1-0: specify the amount of non-overlap SDT1-0: set amount of source delay EQ1-0: equalizing period setting DVI1-0: division ratio of internal clock setting RTN3-0: set the 1-H period
R0Ch	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0	**Power control 3 (R0CH)/** VC2-0:
R0Dh	0	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0	**Power control 4 (R0DH)/** PON: VRL3-0: VRH3-0:
R0Eh	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0	**Power control 5 (R0EH)/** VCOMG: VDV4-0: VCM4-0:

Table 5. Instruction Table 1

INSTRUCTION TABLE

Reg. No	R /W	RS	IB 15	IB 14	IB 13	IB 12	IB 11	IB 10	IB 9	IB 8	IB 7	IB 6	IB 5	IB 4	IB 3	IB 2	IB 1	IB 0	Register Name / Description
R0Fh	0	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0	**Gate scan position (R0FH)/** SCN4-0: scan starting position of gate
R11h	0	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0	**Vertical scroll control (R11H)/** VL7-0:
R14h	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10	**1st screen driving position (R14H)/** SS17-10: 1st screen start position SE17-10: 1st screen end position
R15h	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20	**2nd screen driving position (R15H)/** SS27-20: 2nd screen start position SE27-20: 2nd screen end position
R16h	0	1	HEA7	HEA6	HEA5	HEA4	HEA3	HEA2	HEA1	HEA0	HSA7	HSA6	HSA5	HSA4	HSA3	HSA2	HSA1	HSA0	**Horizontal window address (R16H)/** HEA7-0: Horizontal window address end position HSA7-0: Horizontal window address start position
R17h	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0	**Vertical window Address (R17H)/** VEA7-0: Vertical window address end position VSA7-0: Vertical window address start position
R20h	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0	**Write data Mask (R20H)/** WM15-0: 16-bit Write Data Mask.
R21h	0	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	**RAM address set (R21H)/** AD15-0:16-bit address register
R22h	0	1	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0	**Write data to GRAM (R22H)/** WD15-0:16-bit write data register
	1	1	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	**Read data from GRAM (R22H)/** RD15-0: 16-bit read data register
R23h	0	1	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0	**Write data Mask 18bit (1) (R23H)/** WM17-0: 18-bit compare register
R24h	0	1	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12	**Write data Mask 18bit (2) (R24H)/** WM17-0: 18-bit compare register
R25h	0	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0	**Compare register 18bit (1) (R25H)/** CP17-0: 18-bit compare register
R26h	0	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12	**Compare register 18bit (2) (R26H)/** CP17-0: 18-bit compare register
R30h	0	1	0	0	0	0	0	PKP12	PKP11	PKP10	0	0	0	0	0	PKP02	PKP01	PKP00	**Gamma control 1 (R30H)/** Adjust Gamma voltage
R31h	0	1	0	0	0	0	0	PKP32	PKP31	PKP30	0	0	0	0	0	PKP22	PKP21	PKP20	**Gamma control 2 (R31H)/** Adjust Gamma voltage
R32h	0	1	0	0	0	0	0	PKP52	PKP51	PKP50	0	0	0	0	0	PKP42	PKP41	PKP40	**Gamma control 3 (R32H)/** Adjust Gamma voltage
R33h	0	1	0	0	0	0	0	PRP12	PRP11	PRP10	0	0	0	0	0	PRP02	PRP01	PRP00	**Gamma control 4 (R33H)/** Adjust Gamma voltage
R34h	0	1	0	0	0	0	0	PKN12	PKN11	PKN10	0	0	0	0	0	PKN02	PKN01	PKN00	**Gamma control 5 (R34H)/** Adjust Gamma voltage
R35h	0	1	0	0	0	0	0	PKN32	PKN31	PKN30	0	0	0	0	0	PKN22	PKN21	PKN20	**Gamma control 6 (R35H)/** Adjust Gamma voltage
R36h	0	1	0	0	0	0	0	PKN52	PKN51	PKN50	0	0	0	0	0	PKN42	PKN41	PKN40	**Gamma control 7 (R36H)/** Adjust Gamma voltage
R37h	0	1	0	0	0	0	0	PRN12	PRN11	PRN10	0	0	0	0	0	PRN02	PRN01	PRN00	**Gamma control 8 (R37H)/** Adjust Gamma voltage
R3Ah	0	1	0	0	0	VRP14	VRP13	VRP12	VRP11	VRP10	0	0	0	0	VRP03	VRP02	VRP01	VRP00	**Gamma control 9 (R3AH)/** Adjust Gamma voltage
R3Bh	0	1	0	0	0	VRN14	VRN13	VRN12	VRN11	VRN10	0	0	0	0	VRN03	VRN02	VRN01	VRN00	**Gamma control 10 (R3BH)/** Adjust Gamma voltage
R3Ch	Reserved																		
R3Dh	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VFB2	VFB1	VFB0	**PWM control 1 (R3DH)/** Adjust PWM Feed Back voltage
R3Eh	0	1	0	0	0	0	0	0	0	0	0	0	FPWM2	FPWM1	FPWM0	DPWM2	DPWM1	DPWM0	**PWM control 2 (R3EH)/** Adjust PWM Frequency and PWM Duty
R3Fh	0	1	0	0	0	0	0	0	0	0	0	0	0	EFSM	IBZ	CFSM2	CFSM1	CFSM0	**FSM Control 3 (R3FH)/** Adjust FSM clock cycle, immediately back to zero duty and enable FSM
R50h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OPF	**Power Control (2) (R04H) /** Control voltage detector, OPF

Table 6. Instruction Table 2

INSTRUCTION DESCRIPTIONS

Index

The index instruction specifies the RAM control indexes (R00h to R50h). It sets the register number in the range of 0000000 to 1111111 in binary form. However, R40 to R44 are disabled since they are test registers.

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
IR	0	0	*	*	*	*	*	*	*	*	*	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Status Read

The status read instruction read out the internal status of the IC.

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
SR	1	0	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	0

Start Oscillation (R00h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R00h	0	1	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	1
	1	1	0	0	1	1	1	0	0	1	0	0	0	1	0	1	0	1

The start oscillation instruction restarts the oscillator from the Halt State in the standby mode. After this instruction, wait at least 10 ms for oscillation to stabilize before giving the next instruction. (See the Standby Mode section)

If this register is read forcibly, *3915h is read.

Driver Output Control (R01h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R01h	0	1	0	0	0	0	0	SM	GS	SS	0	0	0	NL4	NL3	NL2	NL1	NL0

GS: Selects the output shift direction of the gate driver. When GS = 0, G1 shifts to G176. When GS = 1, G176 shifts to G1.

SM: Select the division-drive method of the gate driver. When SM = 0, even/odd division is selected; SM = 1, upper/lower division drive is selected. Various connections between TFT panel and the IC can be supported with the combination of SM and GS bit.

SS: Selects the output shift direction of the source driver. When SS = 0, S1 shifts to S396. When SS = 1, S396 shifts to S1. In addition, SS and BGR bits should be specified in case of the RGB order is changed. When SS = 0 and BGR = 0, <R><G><B> are assigned in order from S1 pin. When SS = 1 and BGR = 1, <R><G><B> are assigned in order from S396. Re-write data to GRAM whenever SS and BGR bit are changed.

NL4–0: Specify the number of raster-rows to be driven. The number of raster-row can be adjusted in units of eight. GRAM address mapping is independent of this setting. The set value should be higher than the panel size.

NL4- 0	Display size	Number of LCD driver lines	Gate driver used
0 0 0 0 0	Setting disabled	Setting disabled	Setting disabled
0 0 0 0 1	396 X 16 dots	16	G1 to G16
0 0 0 1 0	396 X 24 dots	24	G1 to G24
0 0 0 1 1	396 X 32 dots	32	G1 to G32
0 0 1 0 0	396 X 40 dots	40	G1 to G40
0 0 1 0 1	396 X 48 dots	48	G1 to G48
0 0 1 1 0	396 X 56 dots	56	G1 to G56
0 0 1 1 1	396 X 64 dots	64	G1 to G64
0 1 0 0 0	396 X 72 dots	72	G1 to G72
0 1 0 0 1	396 X 80 dots	80	G1 to G80
0 1 0 1 0	396 X 88 dots	88	G1 to G88
0 1 0 1 1	396 X 96 dots	96	G1 to G96
0 1 1 0 0	396 X 104 dots	104	G1 to G104
0 1 1 0 1	396 X 112 dots	112	G1 to G112
0 1 1 1 0	396 X 120 dots	120	G1 to G120
0 1 1 1 1	396 X 128 dots	128	G1 to G128
1 0 0 0 0	396 X 136 dots	136	G1 to G136
1 0 0 0 1	396 X 144 dots	144	G1 to G144
1 0 0 1 0	396 X 152 dots	152	G1 to G152
1 0 0 1 1	396 X 160 dots	160	G1 to G160
1 0 1 0 0	396 X 168 dots	168	G1 to G168
1 0 1 0 1	396 X 176 dots	176	G1 to G176

Table 7. NL bit and Drive Duty (SCN4-0=00000)

NOTE: A FP (front porch) and BP (back porch) period will be inserted as blanking period (All gates output Vgoff level) before / after the driver scan through all of the scans.

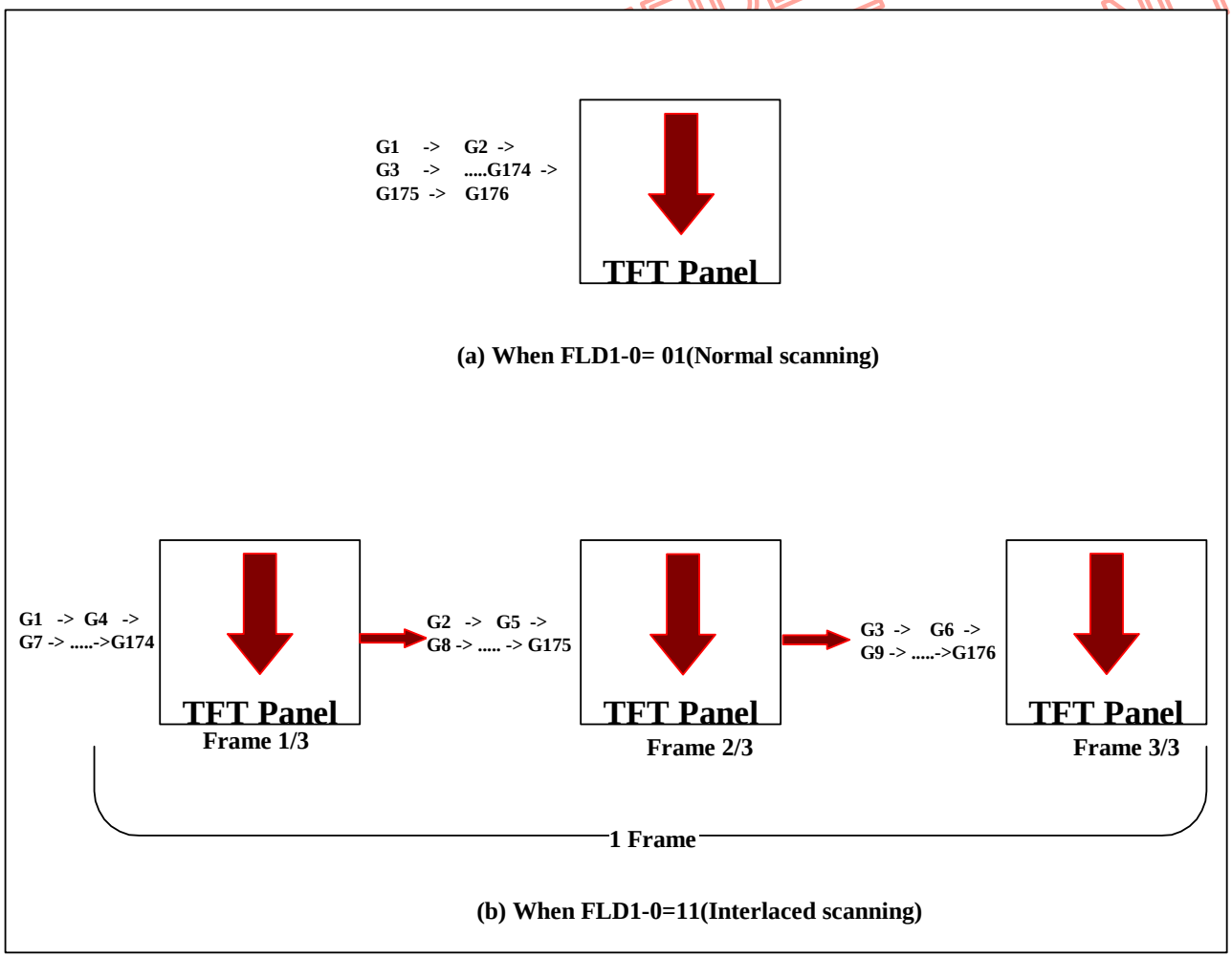
LCD-Driving-Waveform Control (R02h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R02h	0	1	0	0	0	0	FLD1	FLD0	B/C	EOR	0	0	NW5	NW4	NW3	NW2	NW1	NW0

FLD1-0: These bits are for the set up of the interlaced driver's n raster-row. See the following table and figure for the set up value and field raster-row and scanning method.

FLD1	FLD0	Scanning Method
0	0	Setup disabled
0	1	1 field
1	0	Setup disabled
1	1	3 field(interlaced)

Table 8. Association chart for scanning FLD1-0 and n raster-row



n raster-row interlaced scanning method

B/C: When B/C = 0, a B-pattern waveform is generated and alternates at every frame. When B/C = 1, an n raster-row AC waveform is generated and alternates in each raster-row specified by bits EOR and NW5–NW0 in the LCD-driving-waveform control register (R02h). For details, see the n-raster-row Reversed AC Drive section.

EOR: When the C-pattern waveform is set (B/C = 1) and EOR = 1, the odd/even frame-select signals and the n raster-row reversed signals are EORed(Exclusive-OR) for alternating drive. EOR is used when the LCD is not alternated by combining the set values of the number of the LCD drive raster-row and the n raster-row. For details, see the n-raster-row Reversed AC Drive section.

NW5–0: Specify the number of raster-rows that will alternate in the C-pattern waveform setting (B/C = 1). NW5–NW0 alternate for every set value + 1 raster-row, and the first to the 64th raster-rows can be selected.

Entry Mode (R05h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R05h	0	1	0	0	0	BGR	0	0	HWM	0	0	0	I/D1	I/D0	AM	LG2	LG1	LG0

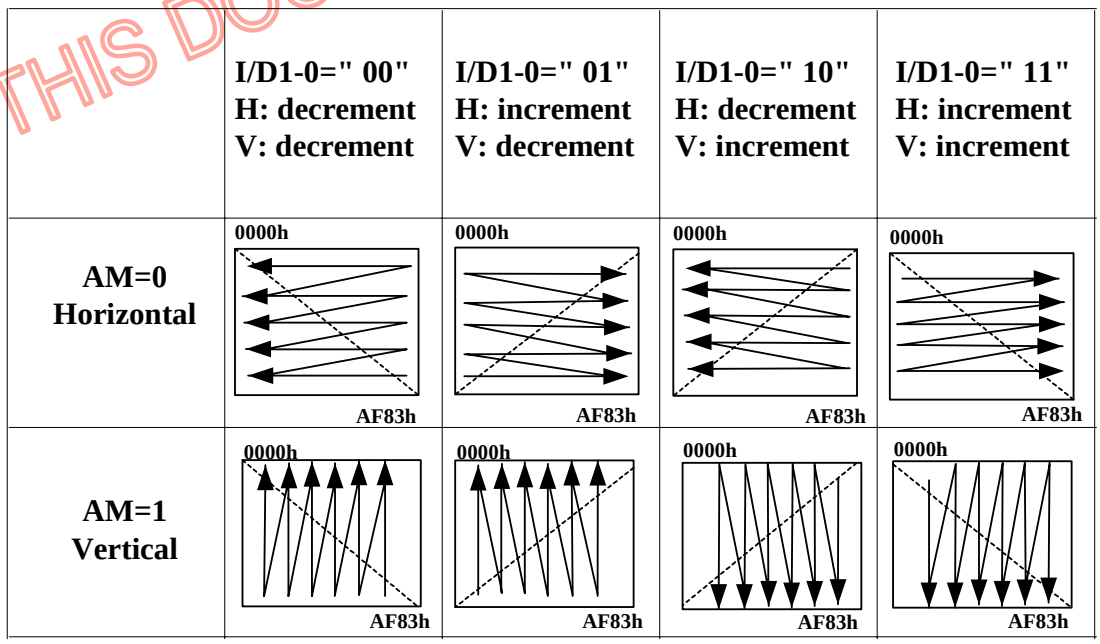
The write date sent from MPU is modified in the NT3915 and written to the GRAM. The display data in the GRAM can be quickly rewritten to reduce the load of the microcomputer software processing. For details, see the Graphics Operation Function section.

BGR: In writing 18-bit data to GRAM, this bit is used to convert the color order. When BGR=1, the order of the color is changed from <R><G><B> to <B><G><R>. Please be aware of the setting BGR to 1 will convert the order of the CP15-0(compare register) and WM15-0(write data mask register) bits in the same way.

HWM: When HWM=1, data can be written to the GRAM at high speed. In high-speed write mode, four words of data are written to the GRAM in a single operation after writing to GRAM four times. Write to RAM four times, otherwise the four words cannot be written to the GRAM. Thus, set the lower 2 bits to 0 when setting the RAM address. For details, see the High-Speed RAM Write Mode section.

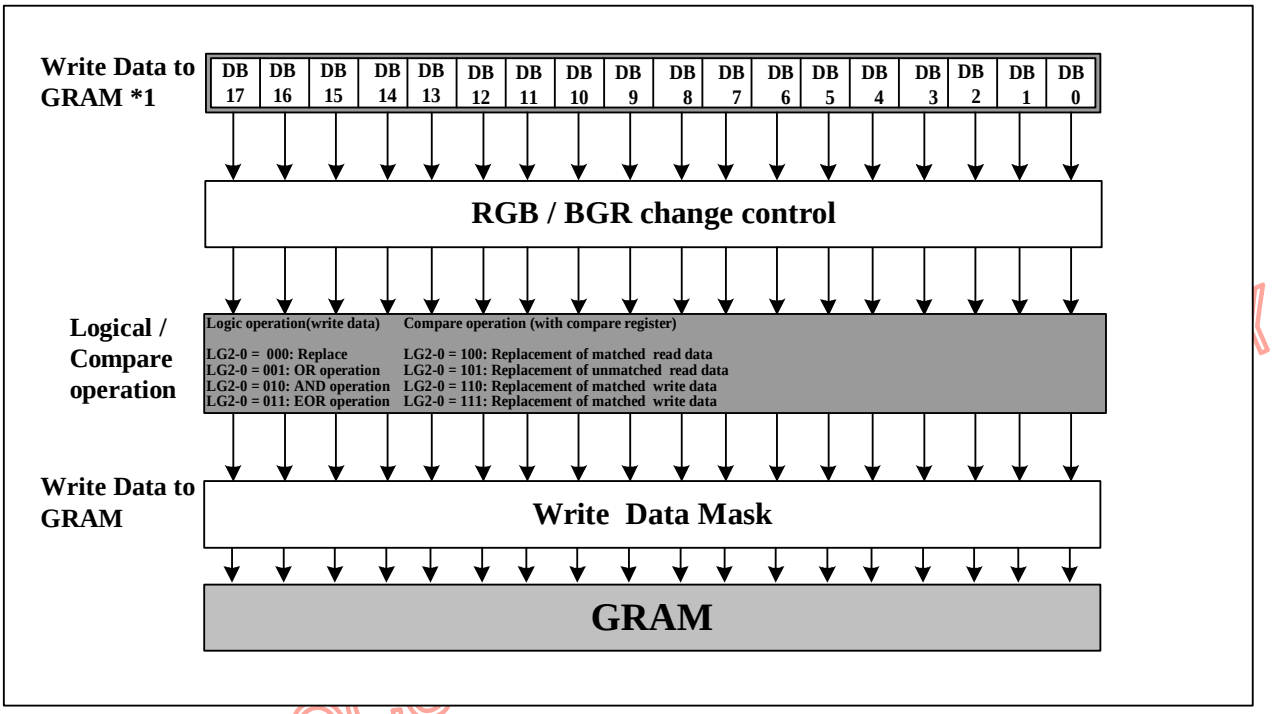
I/D1-0: When I/D1-0 = 1, the address counter (AC) is automatically increased by 1 after the data is written to the GRAM. When I/D1-0 = 0, the AC is automatically decreased by 1 after the data is written to the GRAM. Automatic address counter updating is not performed when reading data from GRAM. The increment/decrement setting of the address counter by I/D1-0 bits is performed independently for the upper (AD15-8) and lower (AD7-0) addresses. The AM bit sets the direction of moving through the addresses when the GRAM is written.

AM: Set the automatic update method of the AC after the data is written to the GRAM. When AM = 0, the data is continuously written in parallel. When AM = 1, the data is continuously written vertically. When window address range is specified, the GRAM in the window address range can be written to according to the I/D1-0 and AM settings.



Adderss Direction Setting

LG2–0: Compare the data read from the GRAM by the microcomputer with the compare registers (CP15–0 or CP17-0) by a compare/logical operation and write the results to GRAM. For details, see the Logical/Compare Operation Function.



RGB swapping and Logical / compare operation

Compare Register 16-bit (R06h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R06h	0	1	CP15	CP14	CP13	CP12	CP11	CP10	CP9	CP8	CP7	CP6	CP5	CP4	CP3	CP2	CP1	CP0

CP15–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer. This register is valid only in the 16-/8-bit interface. For 18-/9-bit interface, use another register suggested below.

Compare Register 18bit - (1) (R25h)
Compare Register 18bit - (1) (R26h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R25h	0	1	0	0	CP11	CP10	CP9	CP8	CP7	CP6	0	0	CP5	CP4	CP3	CP2	CP1	CP0
R26h	0	1	0	0	0	0	0	0	0	0	0	0	CP17	CP16	CP15	CP14	CP13	CP12

CP17–0: Set the compare register for the compare operation with the data read from the GRAM or written by the microcomputer. When 18-/9-bit interface is in use, bit-wise data compare is performed by this register.

Display Control (R07h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R07h	0	1	0	0	0	PT1	PT0	VLE2	VLE1	SPT	0	0	GON	DTE	CL	REV	D1	D0

PT1-0: Normalize the source outputs when non-displayed area of the partial display is driven.

PT1	PT0	Source Output for Non-display Area		Gate Output for Non-display Area
		Positive Polarity	Negative Polarity	Gate driver used
0	0	V63	V0	Normal Drive
0	1	V63	V0	Vgoff
1	0	VSS	VSS	Vgoff
1	1	Hi-Z	Hi-Z	Vgoff

VLE2–1: When VLE1 = 1, a vertical scroll is performed in the 1st screen. When VLE2 = 1, a vertical scroll is performed in the 2nd screen. Vertical scrolling on the two screens cannot be controlled at the same time.

VLE2	VLE1	2nd Screen	1st Screen
0	0	Fixed display	Fixed display
0	1	Fixed display	Scroll
1	0	Scroll	Fixed display
1	1	Setting disabled	Setting disabled

SPT: When SPT = 1, the 2-division LCD drive is performed. For details, see the Screen-division Driving Function section.

GON: Gate off level is set to be VSS when GON = 0.
When GON= 0 and DISPTMG= 0, G1 to G176 output is fixed to VGH level. When GON= 1, G1 to G176 output is fixed to VGH or Vgoff level. See the instruction set up flow for further description on the display on/off flow.

DTE: DISPTMG output is fixed to VSS when DTE = 0.

GON	Gate output
0	VGH
1	VGH/ Vgoff

DTE	DISPTMG output
0	Halt(VSS)
1	Operation (VDD/VSS)

CL: CL = 1 selects 8-color display mode. For details, see the section on 8-color display mode.

CL	Number of display colors
0	262,144 colors
1	8 colors

REV: Displays all character and graphics display sections with reversal when REV = 1. For details, see the Reversed Display Function section. Since the grayscale level can be reversed, display of the same data is enabled on normally white and normally black panels.

1) Combination with the PT1-0 bit

REV	GRAM data	Source output level							
		Display Area		Non-display Area					
				PT1-0=(0,*)		PT1-0=(1,0)		PT1-0=(1,1)	
		Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative
0	16'h0000 : 16'hFFFF	V63 : V0	V0 : V63	V63	V0	VSS	VSS	Hi-Z	Hi-Z
1	16'h0000 : 16'hFFFF	V0 : V63	V63 : V0	V63	V0	VSS	VSS	Hi-Z	Hi-Z

2) Combination with D1-0 bit

		Source output level							
		D1-0=(1,1)		D1-0=(1,0)		D1-0=(0,1)		D1-0=(0,0)	
		Positive	Negative	Positive	Negative	Positive	Negative	Positive	Negative
0	16'h0000 : 16'hFFFF	V63 : V0	V0 : V63	V63	V0	VSS	VSS	VSS	VSS
1	16'h0000 : 16'hFFFF	V0 : V63	V63 : V0	V63	V0	VSS	VSS	VSS	VSS

D1–0: Display is on when D1 = 1 and off when D1 = 0. When off, the display data remains in the GRAM, and can be re-displayed instantly by setting D1 = 1. When D1 is 0, the display is off with the entire source outputs set to the VSS level. Because of this, the NT3915 can control the charging current for the LCD with AC driving. When D1–0 = 01, the internal display of the NT3915 is performed although the display is off. When D1-0 = 00, the internal display operation halts and the display is off.
Control the display on/off while control GON and DTE. For details, see the Instruction Set Up Flow.

GON	DTE	D1	D0	Display Operation	Source output	Gate output
0	0	0	0	Halt	VSS	VGH
0	0	0	1	Operation	VSS	VGH
1	0	0	1	Operation	VSS	Vgoff
1	0	1	1	Operation	Grayscale level output	Vgoff
1	1	1	1	Operation	Grayscale level output	Gate selective line: VGH Gate non-selective line: Vgoff

Notes:
1. Writing from MCU to GRAM is independent from D1–0.
2. In sleep and standby mode, D1–0 = 00. However, the register contents of D1–0 are not modified.

Frame Cycle Control (R0Bh)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R0Bh	0	1	NO1	NO0	SDT1	SDT0	EQ1	EQ0	DIV1	DIV0	0	0	0	0	RTN3	RTN2	RTN1	RTN0

RTN3-0: Set the 1H period (1 raster-row).

RTN3-0	Clock cycles per raster row
0 0 0 0	16
0 0 0 1	17
0 0 1 0	18
: :	: :
1 1 1 0	30
1 1 1 1	31

DIV1-0: Set the division ratio of clocks for internal operation (DIV1-0). Internal operations are driven by clocks, which are frequency divided according to the DIV1-0 setting. Frame frequency can be adjusted along with the 1H period (RTN3-0). When changing number of the drive cycle, adjust the frame frequency. For details, see the Frame Frequency Adjustment Function section.

DIV1	DIV0	Division Ratio	Internal operation clock frequency
0	0	1	fosc/1
0	1	2	fosc/2
1	0	4	fosc/4
1	1	8	fosc/8

$$\text{Frame Frequency} = \frac{\text{fosc}}{\text{Clock cycles per raster-row x division ratio x (line + 8)}} \quad \text{[Hz]}$$

fosc: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit

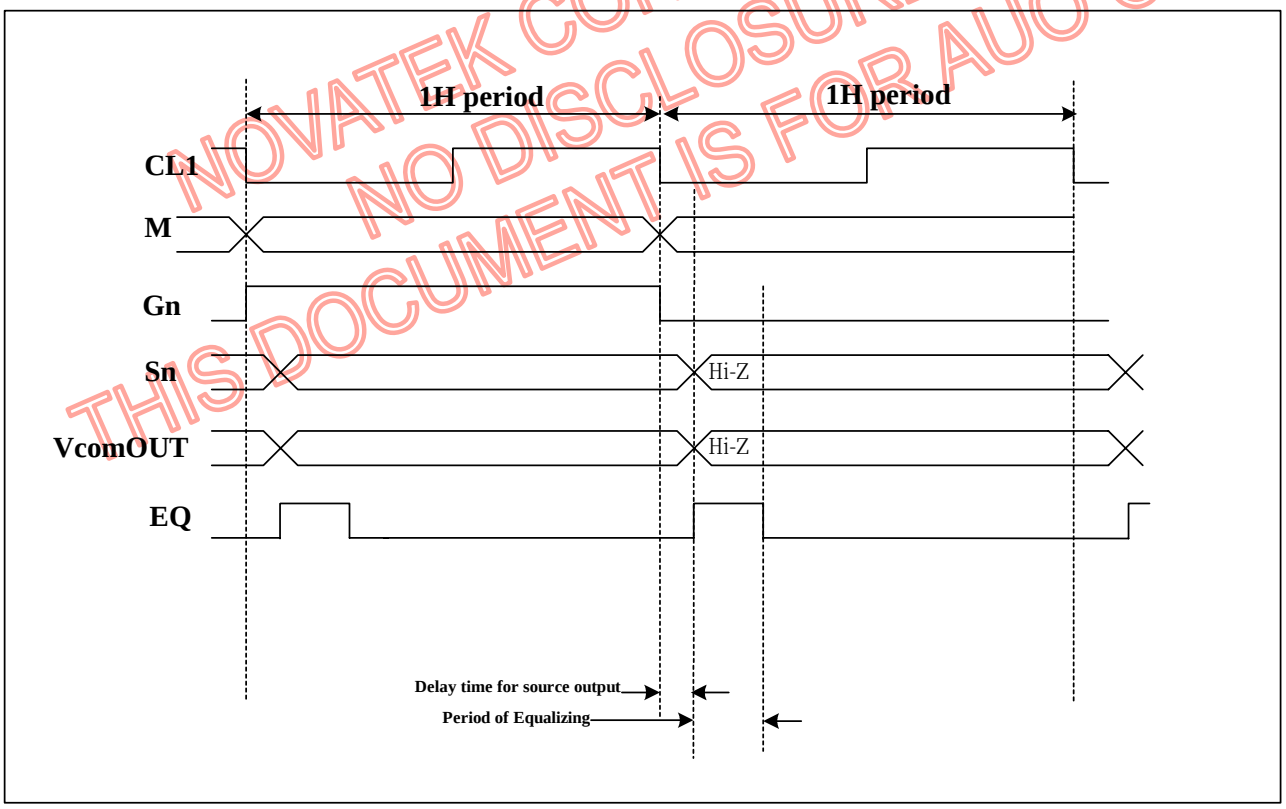
formula for the frame frequency

EQ1-0: EQ period is sustained for the number of clock cycle which is set on EQ1-0. When VcomL<0, set these bits as “00” for preventing the abnormal function.

EQ1	EQ0	EQ period
0	0	No EQ
0	1	1 clock cycle
1	0	2 clock cycle
1	1	3 clock cycle

SDT1-0: Set delay amount from gate edge (end) to source output.

SDT1	SDT0	Delay amount of the source output
0	0	1 clock cycle
0	1	2 clock cycle
1	0	3 clock cycle
1	1	4 clock cycle



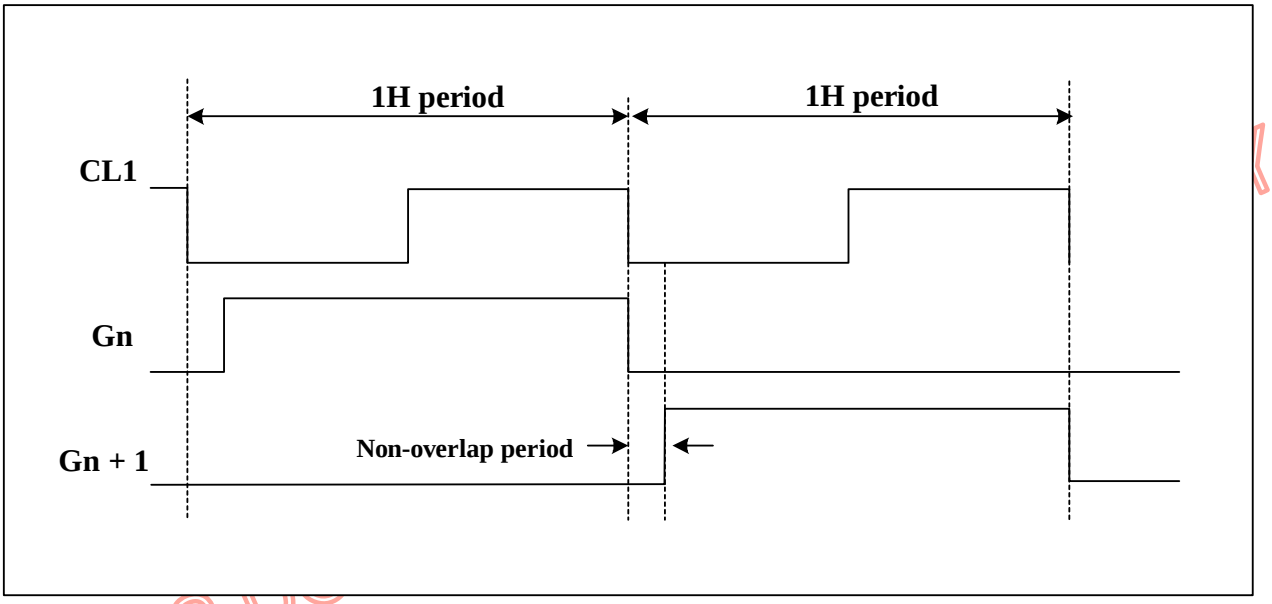
Set Delay from Gate Output to Sucrce Output and EQ signal

Note: All source driver’s pins output Hi-Z level, and they are shorted to VCOMOUT pin.

NO1-0: Set amount of non-overlay for the gate output.

NO1	NO0	Amount of non-overlap
0	0	1 clock cycle
0	1	4 clock cycle
1	0	6 clock cycle
1	1	8 clock cycle

Note: The amount of non-overlap time is defined from the falling edge of the CL1



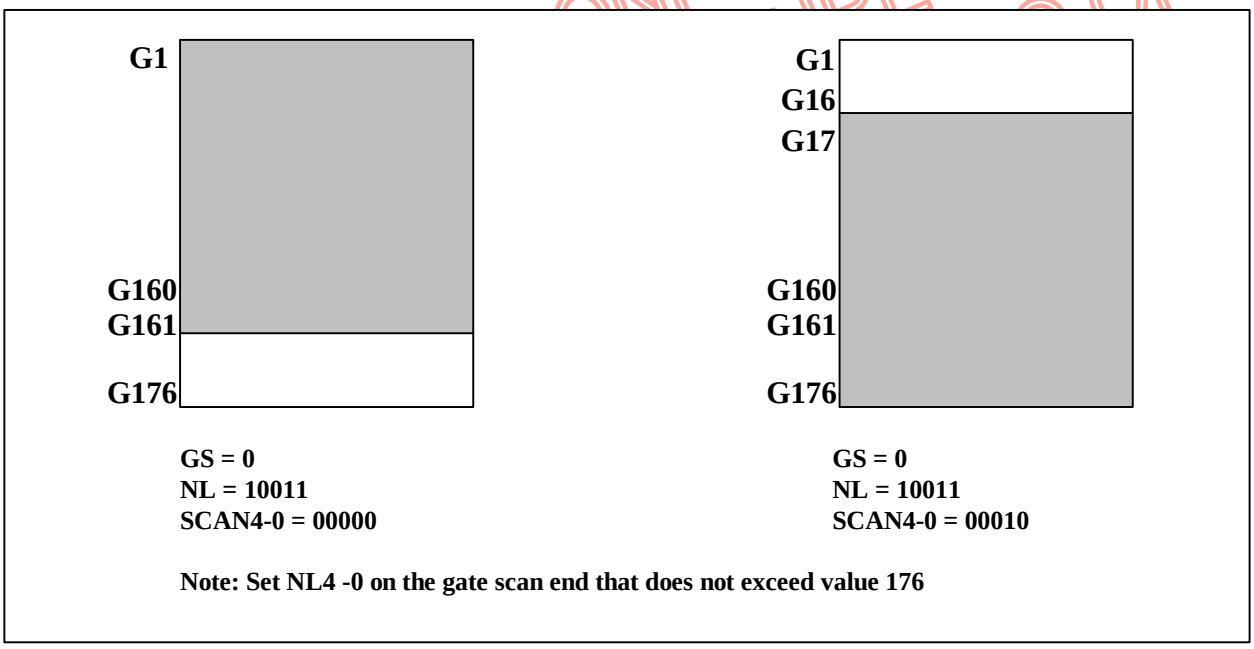
Non-overlap period

Gate Scan Position (R0Fh)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R0Fh	0	1	0	0	0	0	0	0	0	0	0	0	0	SCN4	SCN3	SCN2	SCN1	SCN0

SCN 4-0: Set the scanning starting position of the gate driver.

SCN4-0	Scanning start position	
	GS=0	GS=1
0 0 0 0 0	G1	G176
0 0 0 0 1	G9	G168
0 0 0 1 0	G17	G160
:	:	:
1 0 0 1 1	G153	G24
1 0 1 0 0	G161	G16
1 0 1 0 1	G169	G8



Relationship between NL and SCN set up value

Vertical Scroll Control (R11h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R11h	0	1	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0

VL7-0: Specify scroll length at the scroll display for vertical smooth scrolling. Any raster-row from the first to 176th can be scrolled for the number of the raster-row. After 176th raster-row is displayed, the display restarts from the first raster-row. The display-start raster-row (VL7-0) is valid when VLE1 = 1 or VLE2 = 1. The raster-row display is fixed when VLE2-1 = 00.

VL7- 0	Scroll length
0 0 0 0 0 0 0 0	0 raster-row
0 0 0 0 0 0 0 1	1 raster-row
0 0 0 0 0 0 1 0	2 raster-row
⋮	⋮
1 0 1 0 1 1 1 0	174 raster-row
1 0 1 0 1 1 1 1	175 raster-row

Note: Don't set any higher raster-row than 175 ("AF"H)

1st Screen Driving Position (R14h)
2nd Screen Driving Position (R15h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R14h	0	1	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10
R15h	0	1	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

SS17–10: Specify the driving start position for the first screen in a line unit. The LCD driving starts from the 'set value+1' gate driver.

SE17–10: Specify the driving end position for the first screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SS17–10 = 07h and SE17–10 = 10h are set, the LCD driving is performed from G8 to G17, and non-display driving is performed for G1 to G7, G18, and others. Ensure that SS17–10 ≤ SE17–10 ≤ AFh. For details, see the Screen-division Driving Function section.

SS27–20: Specify the driving start position for the second screen in a line unit. The LCD driving starts from the 'set value + 1' gate driver. The second screen is driven when SPT = 1.

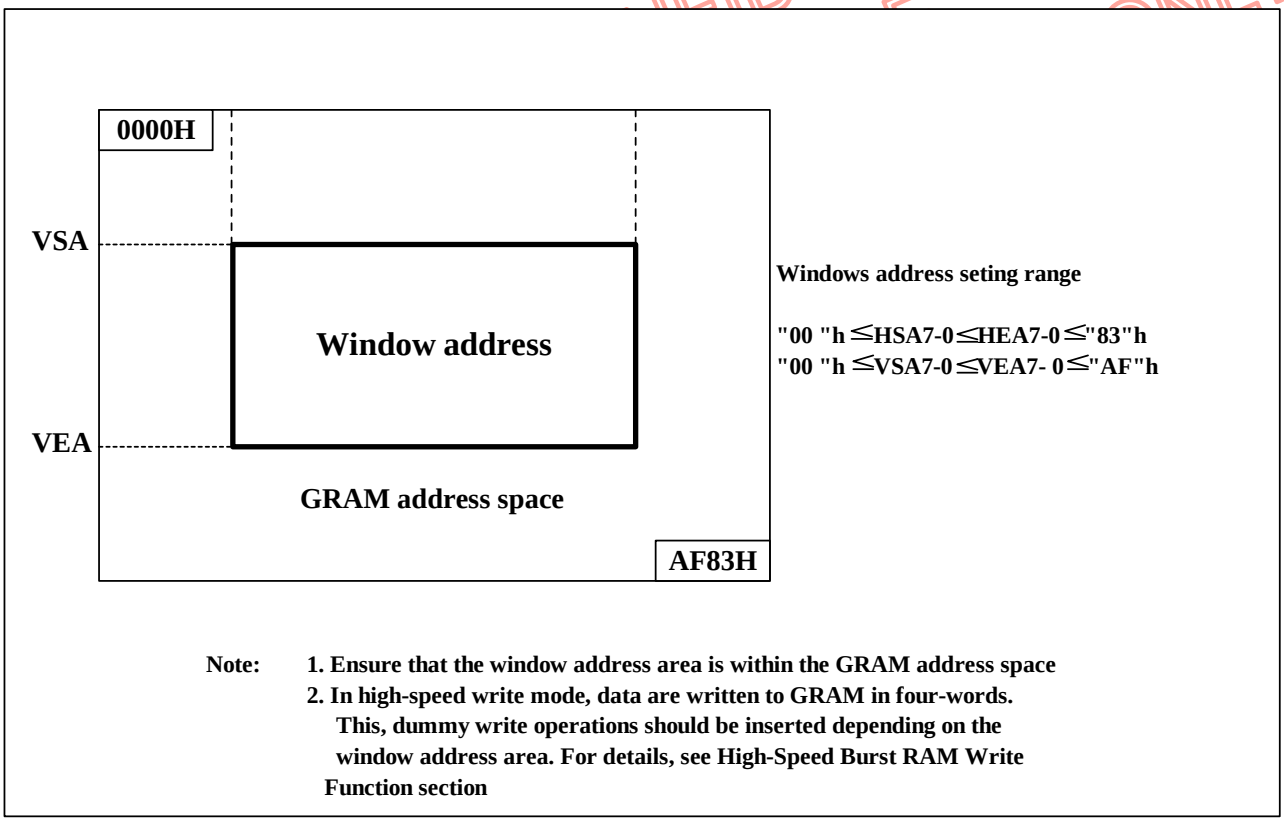
SE27–20: Specify the driving end position for the second screen in a line unit. The LCD driving is performed to the 'set value + 1' gate driver. For instance, when SPT = 1, SS27–20 = 20h, and SE27–20 = 4Fh are set, the LCD driving is performed from G33 to G80. Ensure that SS17–10 ≤ SE17–10 ≤ SS27–20 ≤ SE27–20 ≤ AFh. For details, see the Screen-division Driving Function section.

Horizontal RAM Address Position (R16h)
Vertical RAM Address Position (R17h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R16h	0	1	HEA 7	HEA 6	HEA 5	HEA 4	HEA 3	HEA 2	HEA 1	HEA 0	HSA 7	HSA 6	HSA 5	HSA 4	HSA 3	HSA 2	HSA 1	HSA 0
R17h	0	1	VEA7	VEA6	VEA5	VEA4	VEA3	VEA2	VEA1	VEA0	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0

HSA7-0/HEA7-0: Specify the horizontal start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by HEA 7-0 from the address specified by HSA7-0. Note that an address must be set before RAM is written. Ensure 00h ≤ HSA7-0 ≤ HEA7-0 ≤ 83h.

VSA7-0/VEA7-0: Specify the vertical start/end positions of a window for access in memory. Data can be written to the GRAM from the address specified by VEA7-0 from the address specified by VSA7-0. Note that an address must be set before RAM is written. Ensure 00h ≤ VSA7-0 ≤ VEA7-0 ≤ AFh.



Windows address setting range

Power Control 1 (R03h)
Power Control 2(OP-Amp Control) (R50h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R03h	0	1	0	0	0	0	OPF	BT2	BT1	BT0	DC2	DC1	DC0	AP2	AP1	AP0	SLP	STB
R50h	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OPF

BT2–0: The output factor of step-up is switched. Adjust scale factor of the step-up circuit by the voltage used. When the step-up operating frequency is high, the driving ability of the step-up circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

BT2- 0	AVDD Output	VGH Output	Notes*
0 0 0	2 X VCI1	3 X VCI2	VGH = VCI1 X 6 times
0 0 1	2 X VCI1	4 X VCI2	VGH = VCI1 X 8 times
0 1 0	3 X VCI1	3 X VCI2	VGH = VCI1 X 9 times
0 1 1	3 X VCI1	2 X VCI2	VGH = VCI1 X 6 times
1 0 0	2 X VCI1	VCI1 + 2 X VCI2	VGH = VCI1 X 5 times
1 0 1	2 X VCI1	VCI1 + 3 X VCI2	VGH = VCI1 X 7 times
1 1 0	Step-up stopped	3 X VCI2	VGH = VCI2 X 3 times
1 1 1	Setting disabled	Setting disabled	Setting disabled

Note: The step-up factors of VGH are derived from VCI1 when AVDD and VCI2 are shorted. The conditions of AVDD $\leq$ 5.5V and VGH $\leq$ 15.0V must be satisfied.

DC2-0: The operating frequency in the charge-pump circuit is selected. When the charge-pump operating frequency is high, the driving ability of the charge-pump circuit and the display quality become high, but the current consumption is increased. Adjust the frequency considering the display quality and the current consumption.

DC2- 0	Step-up Cycle in Charge-pump Circuit1	Step-up Cycle in Charge-pump Circuit 2/3/4
0 0 0	DCCLK / 1	DCCLK / 4
0 0 1	DCCLK / 2	DCCLK / 4
0 1 0	DCCLK / 4	DCCLK / 4
0 1 1	DCCLK / 2	DCCLK / 16
1 0 0	DCCLK / 1	DCCLK / 8
1 0 1	DCCLK / 2	DCCLK / 8
1 1 0	DCCLK / 4	DCCLK / 8
1 1 1	DCCLK / 4	DCCLK / 16

AP2–0: The amount of fixed current in the operational amplifier for the power supply can be adjusted. When the amount of fixed current is large, the LCD driving ability and the display quality become high, but the current consumption is increased. Adjust the fixed current considering the display quality and the current consumption. During no display, when AP2-0 = “000”, the current consumption can be reduced by ending the operational amplifier and charge-pump circuit operation.

AP2	AP1	AP0	Amount of Current in Operational Amplifier
0	0	0	Operation of the operational amplifier and charge-pump circuit stops.
0	0	1	Small
0	1	0	Small or medium
0	1	1	Medium
1	0	0	Medium or large
1	0	1	Large
1	1	0	Setting Inhibited
1	1	1	Setting Inhibited

SLP: When SLP = 1, the NT3915 enters the sleep mode, where the internal display operations are halted except for the R-C oscillator, thus reducing current consumption. Only the following instructions can be executed during the sleep mode.

– Power control (BT2–0, DC3–0, AP2–0, SLP, STB, VC2-0, CAD, VRL3-0, PON, VRH3-0, VCOMG, VDV4-0, and VCM4-0 bits)

During the sleep mode, the other GRAM data and instructions cannot be updated although they are retained and G1 to G176 output is fixed to VSS level, and register set-up is protected (maintained).

STB: When STB = 1, the NT3915 enters the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

– Standby mode cancel (STB = “0”)
– Start oscillation

During the standby mode, the GRAM data and instructions may be lost. To prevent this, they must be set again after releasing from the standby mode.

OPF: When OPF = 1, the NT3915 enters the power saving mode, where the operational amplifier operation completely stops, halting all source driver outputs in the non-overlap region for the gate output.

Power Control 3 (R0Ch)
Power Control 4 (R0Dh)
Power Control 5 (R0Eh)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R0Ch	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	VC2	VC1	VC0
RODh	0	1	0	0	0	0	VRL3	VRL2	VRL1	VRL0	0	0	0	PON	VRH3	VRH2	VRH1	VRH0
R0Eh	0	1	0	0	VCOMG	VDV4	VDV3	VDV2	VDV1	VDV0	0	0	0	VCM4	VCM3	VCM2	VCM1	VCM0

VC2-0: Adjust reference voltage of GVDD, VGOFF and VCI1 to optional rate of Vci. Also, when VC2-0 = “111”, it is possible to stop the internal reference voltage generator. This leads to optional power on for GVDD/VCI1 with REGP externally.

VC2	VC1	VC0	Internal Reference Voltage (REGP) of GVDD and VCI1
0	0	0	VCI
0	0	1	0.92 X VCI
0	1	0	0.87 X VCI
0	1	1	0.83 X VCI
1	0	0	0.76 X VCI
1	0	1	0.73 X VCI
1	1	0	0.68 X VCI
1	1	1	VCI1: Hi-z, REGP:GND

Note:
1. Leave these settings open because the voltage other than that for halting the internal circuit is output for REGP and REGN.
2. The reference voltage REGN of VGOFF is internal reference.

VRL3-0: Set magnification of amplification for Vgoff voltage. It allows magnifying the amplification of VCI from -1.5 to -6.5 times.

VRL3- 0	Vgoff Voltage	VRL3- 0	Vgoff Voltage
0 0 0 0	VCI X –1.5 times	1 0 0 0	VCI X –5.0 times
0 0 0 1	VCI X –2.0 times	1 0 0 1	VCI X –5.5 times
0 0 1 0	VCI X –2.5 times	1 0 1 1	VCI X –6.0 times
0 0 1 1	VCI X –3.0 times	1 0 1 0	VCI X –6.5 times
0 1 0 0	VCI X –3.5 times	1 1 0 1	Setting disabled
0 1 0 1	VCI X –4.0 times	1 1 0 0	Setting disabled
0 1 1 0	VCI X –4.5 times	1 1 1 0	Setting disabled
0 1 1 1	Stopped	1 1 1 1	Stopped

Note: Adjust VCI and VRL3-0 so that Vgoff voltage is higher than –16.0 V.

PON: This is an operation starting bit for the charge-pump circuit 3. PON=0 is to stop, and PON=1 to start operation.

VRH3-0: Set the amplified factor of the GVDD voltage. It allows to amplify from 1.33 to 2.775 times of REGP input voltage.

VRH3- 0	GVDD Voltage	VRH3- 0	GVDD Voltage
0 0 0 0	REGP X 1.33 times	1 0 0 0	REGP X 1.900 times
0 0 0 1	REGP X 1.45 times	1 0 0 1	REGP X 2.175 times
0 0 1 0	REGP X 1.55 times	1 0 1 1	REGP X 2.325 times
0 0 1 1	REGP X 1.65 times	1 0 1 0	REGP X 2.475 times
0 1 0 0	REGP X 1.75 times	1 1 0 1	REGP X 2.625 times
0 1 0 1	REGP X 1.80 times	1 1 0 0	REGP X 2.700 times
0 1 1 0	REGP X 1.85 times	1 1 1 0	REGP X 2.775 times
0 1 1 1	Stopped	1 1 1 1	Stopped

Note: Adjust VC3-0 and VRH3-0 so that the GVDD voltage is lower than 5.5V

VCOMG: When VCOMG = 1, VcomL voltage can output to negative voltage .
When VCOMG = 0, VcomL voltage becomes VSS. Therefore, low power consumption is accomplished. Also, When VCOMG = 0 and when Vcom is driven in A/C, set up of the VDV4-0 is invalid. In this case, adjustment of Vcom A/C oscillation must be adjusted VcomH with VCM4-0.

VDV4-0: Set the alternating amplitudes of Vcom at the Vcom alternating drive. These bits amplify Vcom and Vgoff 0.6 to 1.23 times the GVDD voltage. When the Vcom alternation is not driven, the settings become invalid.

VDV4- 0	Vcom Amplitude	VDV4- 0	Vcom Amplitude
0 0 0 0 0	GVDD X 0.60	1 0 0 0 1	GVDD X 1.08
0 0 0 0 1	GVDD X 0.63	1 0 0 1 0	GVDD X 1.11
0 0 0 1 0	GVDD X 0.66	1 0 0 1 1	GVDD X 1.14
:	:	1 0 1 0 0	GVDD X 1.17
0 1 1 0 0	GVDD X 0.96	1 0 1 0 1	GVDD X 1.20
0 1 1 0 1	GVDD X 0.99	1 0 1 1 0	GVDD X 1.23
0 1 1 1 0	GVDD X 1.02	1 0 1 1 1	Setting disabled
0 1 1 1 1	Setting disabled	1 1 * * *	Setting disabled
1 0 0 0 0	GVDD X 1.05		

Note: Adjust the settings between GVDD and VDV4-0 so that the Vcom amplitudes are lower than 6.0 V.

VCM4-0: Set the VcomH voltage (a high-level voltage at the Vcom alternating drive). These bits amplify the VcomH voltage 0.4 to 0.98 times the GVDD voltage. When VCM3-0 = “1111”, the adjustment of the internal volume stops, and VcomH can be adjusted from VcomR by an external resistor.

VCM4-0	VcomH Voltage
0 0 0 0 0	GVDD X 0.40 times
0 0 0 0 1	GVDD X 0.42 times
0 0 0 1 0	GVDD X 0.44 times
: :	: :
0 1 1 0 0	GVDD X 0.64 times
0 1 1 0 1	GVDD X 0.66 times
0 1 1 1 0	GVDD X 0.68 times
0 1 1 1 1	The internal volume stops and VcomH can be adjusted from VcomR by an external variable resistor.
1 0 0 0 0	GVDD X 0.70 times
1 0 0 0 1	GVDD X 0.72 times
1 0 0 1 0	GVDD X 0.74 times
: :	: :
1 1 1 0 0	GVDD X 0.94 times
1 1 1 0 1	GVDD X 0.96 times
1 1 1 1 0	GVDD X 0.98 times
1 1 1 1 1	The internal volume stops, and VcomH can be adjusted from VcomR by an external variable resistor.

Note: Adjust the settings between GVDD and VCM4-0 so that the VcomH voltage is lower than GVDD.

RAM Write Data Mask – 16bit (R20h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R20h	0	1	WM15	WM14	WM13	WM12	WM11	WM10	WM9	WM8	WM7	WM6	WM5	WM4	WM3	WM2	WM1	WM0

WM15–0: In writing to the GRAM, these bits mask writing in a bit unit. This register is valid only in the 16-/8-bit interface. For 18-/9-bit interface, use another register suggested below. When WM15 = 1, this bit masks the write data of DB15 and does not write to the GRAM. Similarly, the WM14 to 0 bits mask the write data of DB14 to 0 in a bit unit. For details, see the Graphics Operation Function section.

RAM Write Data Mask 18bit – (1) (R23h)
RAM Write Data Mask 18bit – (2) (R24h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R23h	0	1	0	0	WM11	WM10	WM9	WM8	WM7	WM6	0	0	WM5	WM4	WM3	WM2	WM1	WM0
R24h	0	1	0	0	0	0	0	0	0	0	0	0	WM17	WM16	WM15	WM14	WM13	WM12

WM17–0: In writing to the GRAM, these bits mask writing in a bit unit. This register is valid only in the 18-/9-bit interface. When 18-/9-bit interface is in use, bit-wise data masking is performed by this register.

RAM Address Set (R21h)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R21h	0	1	AD15	AD14	AD13	AD12	AD11	AD10	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0

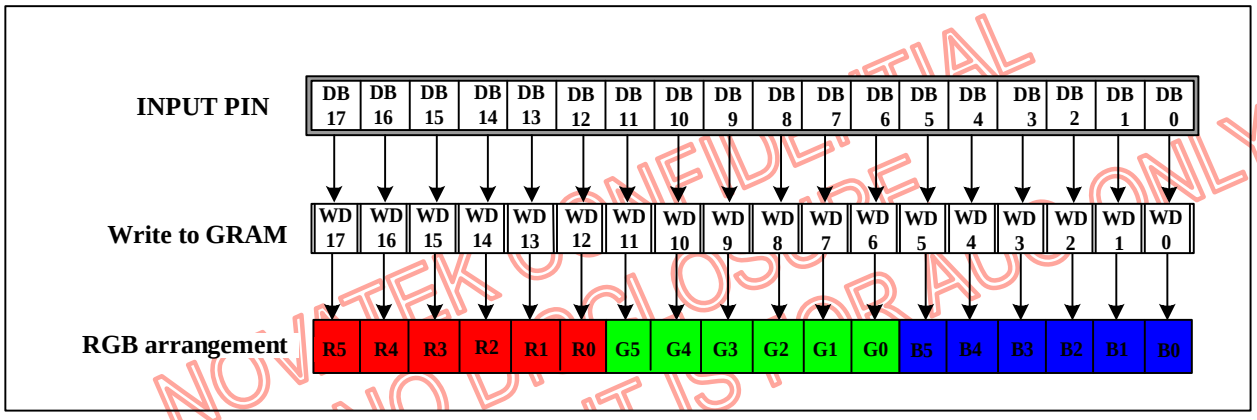
AD15–0: Initially set GRAM addresses to the address counter (AC). Once the GRAM data is written, the AC is automatically updated according to the AM and I/D bit settings. This allows consecutive accesses without resetting address. Once the GRAM data is read, the AC is not automatically updated. GRAM address setting is not allowed in the standby mode. Ensure that the address is set within the specified window address.

AD15 to AD0	GRAM setting
“0000H” to “0083”H	Bitmap data for G1
“0100H” to “0183”H	Bitmap data for G2
“0200H” to “0283”H	Bitmap data for G3
“0300H” to “0383”H	Bitmap data for G4
: :	: :
“AC00H” to “AC83”H	Bitmap data for G173
“AD00H” to “AD83”H	Bitmap data for G174
“AE00H” to “AE83”H	Bitmap data for G175
“AF00H” to “AF83”H	Bitmap data for G176

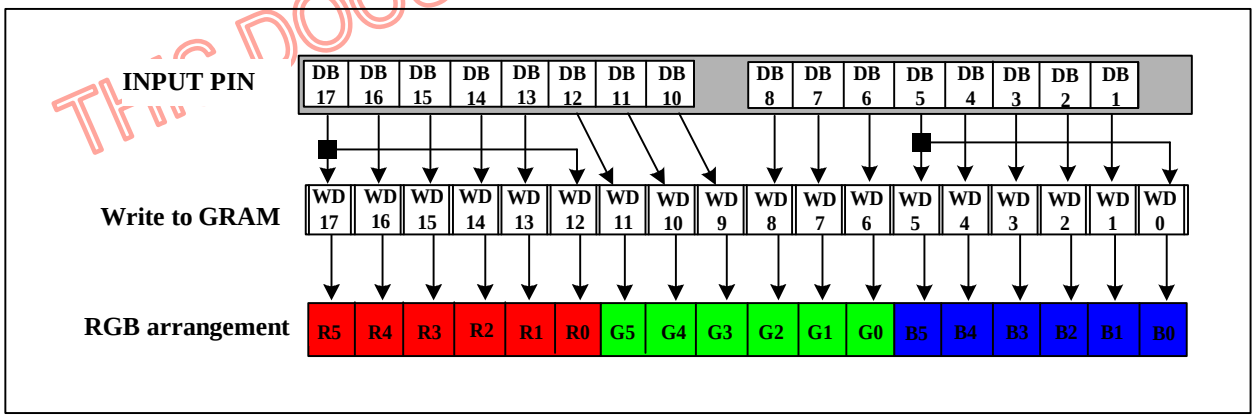
Write Data to GRAM (R22h)

Reg. No	R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R22h	0	1	WD17	WD16	WD15	WD14	WD13	WD12	WD11	WD10	WD9	WD8	WD7	WD6	WD5	WD4	WD3	WD2	WD1	WD0

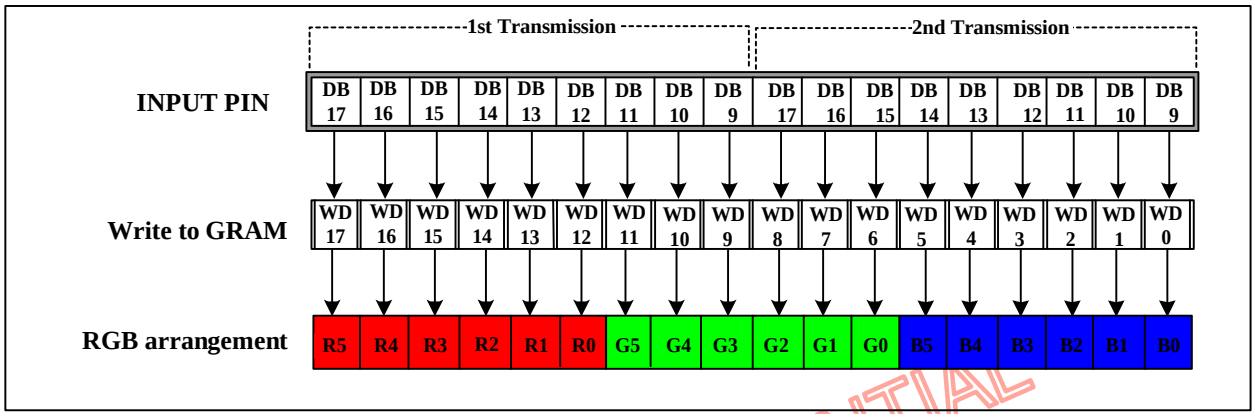
WD17-0: Input data for GRAM can be expanded to 18 bits. The expansion format varies according to the interface method. The input data selects the grayscale level. After a write, the address is automatically updated according to AM and I/D bit settings. The GRAM cannot be accessed in standby mode. When 16-/8-bit interface is in use, the write data is expanded to 18 bits by writing the MSB of the <R><B> data to its LSB.
Pin assignment varies according to the interface method. (see the following figure for more information)



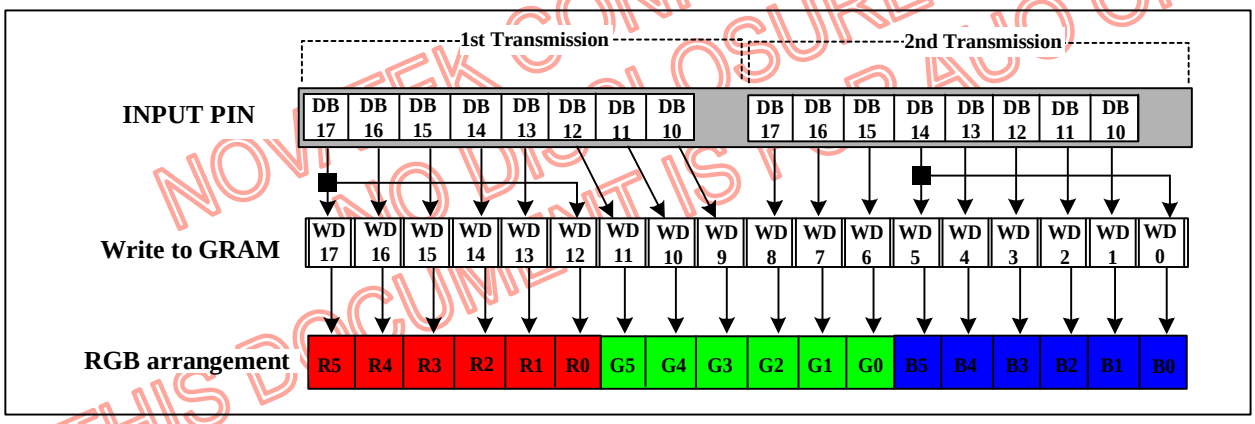
18-bit System interface (260K-color)



16-bit System interface (65K-color)



9-bit System interface (260K-color)



8-bit System interface (65K-color)

GRAM data	Grayscale Polarity		GRAM Data	Grayscale Polarity		GRAM Data	Grayscale Polarity		GRAM Data	Grayscale Polarity	
RGB	N	P	RGB	N	P	RGB	N	P	RGB	N	P
000000	V0	V63	010000	V16	V47	100000	V32	V31	110000	V48	V15
000001	V1	V62	010001	V17	V46	100001	V33	V30	110001	V49	V14
000010	V2	V61	010010	V18	V45	100010	V34	V29	110010	V50	V13
000011	V3	V60	010011	V19	V44	100011	V35	V28	110011	V51	V12
000100	V4	V59	010100	V20	V43	100100	V36	V27	110100	V52	V11
000101	V5	V58	010101	V21	V42	100101	V37	V26	110101	V53	V10
000110	V6	V57	010110	V22	V41	100110	V38	V25	110110	V54	V9
000110	V7	V56	010110	V23	V40	100110	V39	V24	110110	V55	V8
001000	V8	V55	011000	V24	V39	101000	V40	V23	111000	V56	V7
001001	V9	V54	011001	V25	V38	101001	V41	V22	111001	V57	V6
001010	V10	V53	011010	V26	V37	101010	V42	V21	111010	V58	V5
001011	V11	V52	011011	V27	V36	101011	V43	V20	111011	V59	V4
001100	V12	V51	011000	V28	V35	101100	V44	V19	111100	V60	V3
001101	V13	V50	011001	V29	V34	101101	V45	V18	111101	V61	V2
001100	V14	V49	011010	V30	V33	101100	V46	V17	111110	V62	V1
001101	V15	V48	011011	V31	V32	101101	V47	V16	111111	V63	V0

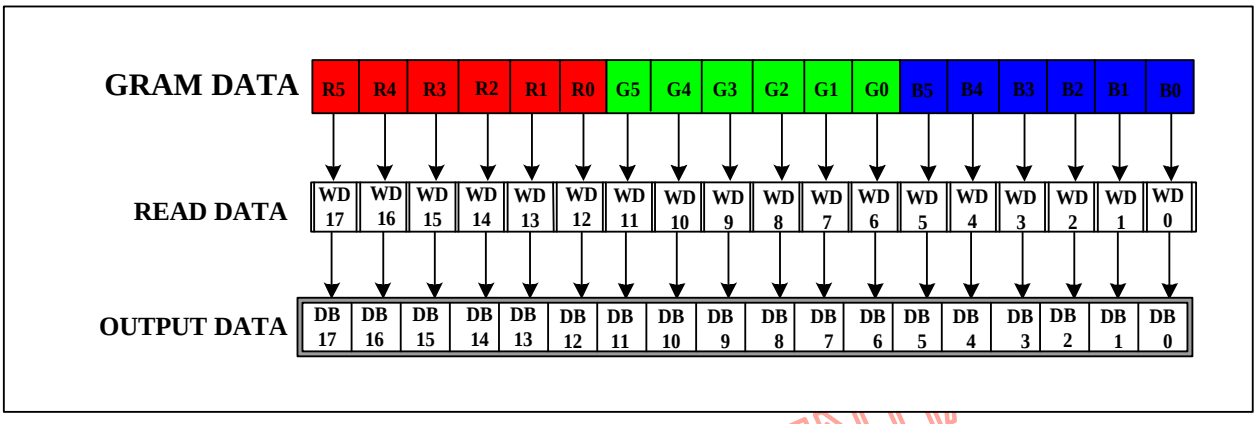
Table 9. GRAM Data and Grayscale Level

Read Data from GRAM (R22h)

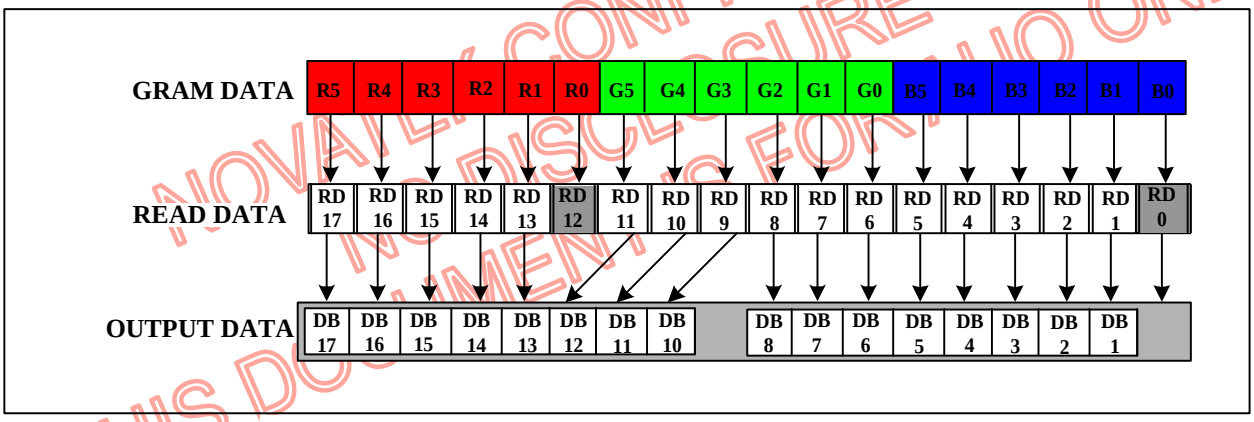
Reg. No	R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R22h	0	1	RD17	RD16	RD15	RD14	RD13	RD12	RD11	RD10	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

RD17–0: Read 18-bit data from the GRAM. When the data is read to the MCU, the first-word read immediately after the GRAM address setting is latched from the GRAM to the internal read-data latch. The data on the data bus (DB17–0) becomes invalid and the second-word read is normal.

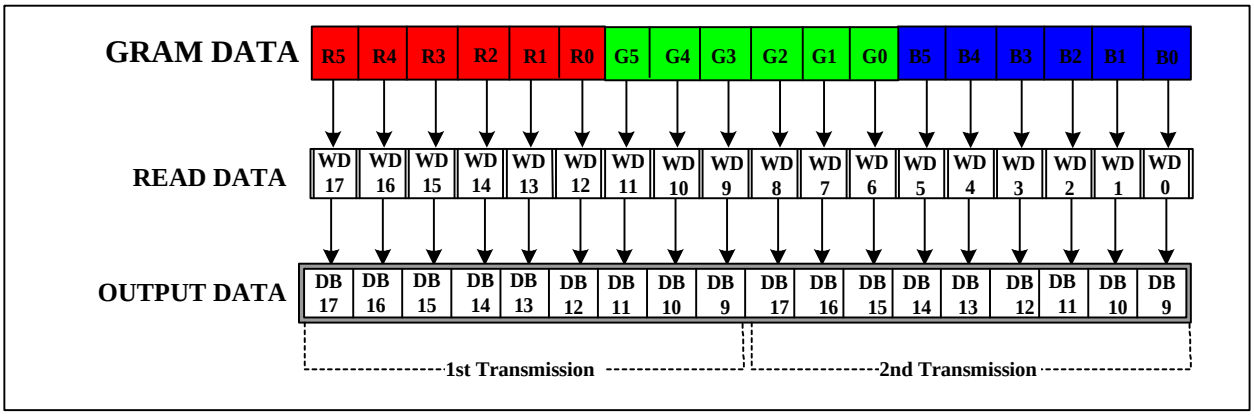
When bit processing, such as a logical operation, is performed within the NT3915, only one read can be processed since the latched data in the first word is used. In case of 16-/8-bit interface, the LSB of <R><B> color data will not be read. Pin assignment varies according to the interface method. (see the following figure for more information)



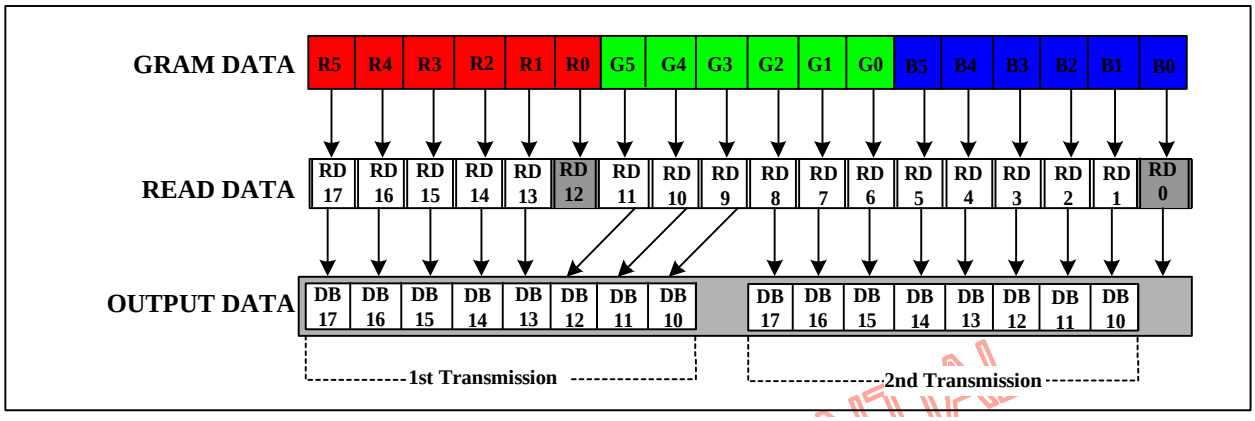
18-bit System interface for GRAM read



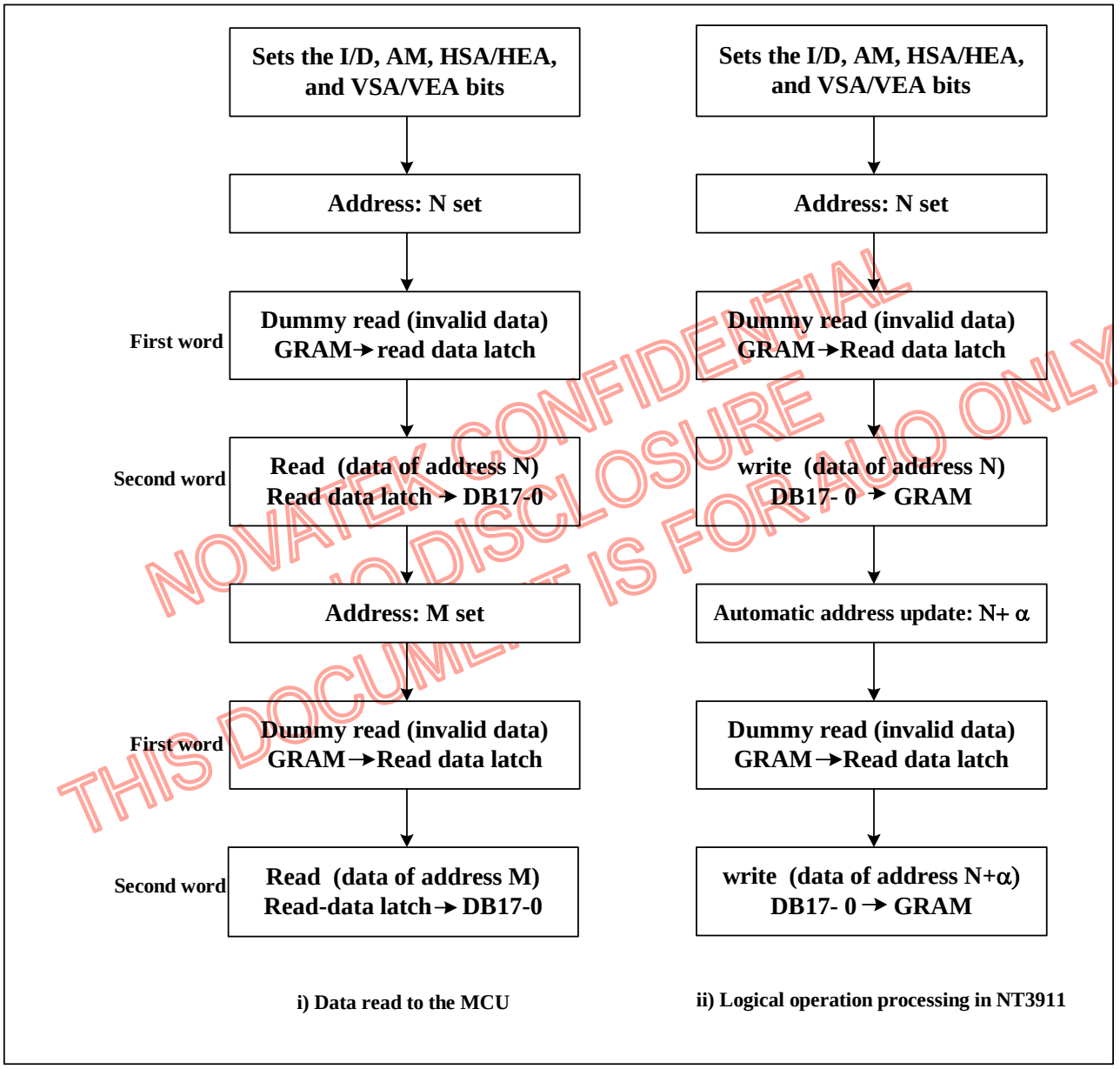
16-bit System interface for GRAM read



9-bit System interface for GRAM read



8-bit System interface for GRAM read



GRAM read sequence

Gamma Control (R30h To R3Bh)

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R30h	0	1	0	0	0	0	0	PKP 12	PKP 11	PKP 10	0	0	0	0	0	PKP 02	PKP 01	PKP 00
R31h	0	1	0	0	0	0	0	PKP 32	PKP 31	PKP 30	0	0	0	0	0	PKP 22	PKP 21	PKP 20
R32h	0	1	0	0	0	0	0	PKP 52	PKP 51	PKP 50	0	0	0	0	0	PKP 42	PKP 41	PKP 40
R33h	0	1	0	0	0	0	0	PRP 12	PRP 11	PRP 10	0	0	0	0	0	PRP 02	PRP 01	PRP 00
R34h	0	1	0	0	0	0	0	PKN 12	PKN 11	PKN 10	0	0	0	0	0	PKN 02	PKN 01	PKN 00
R35h	0	1	0	0	0	0	0	PKN 32	PKN 31	PKN 30	0	0	0	0	0	PKN 22	PKN 21	PKN 20
R36h	0	1	0	0	0	0	0	PKN 52	PKN 51	PKN 50	0	0	0	0	0	PKN 42	PKN 41	PKN 40
R37h	0	1	0	0	0	0	0	PRN 12	PRN 11	PRN 10	0	0	0	0	0	PRN 02	PRN 01	PRN 00
R3Ah	0	1	0	0	0	VRP 14	VRP 13	VRP 12	VRP 11	VRP 10	0	0	0	0	VRP 03	VRP 02	VRP 01	VRP 00
R3Bh	0	1	0	0	0	VRN 14	VRN 13	VRN 12	VRN 11	VRN 10	0	0	0	0	VRN 03	VRN 02	VRN 01	VRN 00

PKP52–00: Gamma micro adjustment register for the positive polarity output

PRP12-00: Gradient adjustment register for the positive polarity output

PKN52-00: Gamma micro adjustment register for the negative polarity output

PRN12-00: Gradient adjustment register for the negative polarity output

VRP14-00: Adjustment register for positive polarity output amplification adjustment

VRN14-00: Adjustment register for negative polarity output amplification adjustment

For details, see the Gamma Adjustment Function.

PWM Control 1 (R3Dh)

Reg. No	R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R3Dh	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	VFB2	VFB1	VFB0

VFB2–0: Control PWM feed back voltage. When VFB2_0=”000” ,stop PWM output. Default=”000”;

VFB2–0	PWM feed back voltage	PWM feed back current(Rfb=30Ω)
000	0V	0mA
001	0.06V	2mA
010	0.3V	10mA
011	0.36V	12mA
100	0.42V	14mA
101	0.48V	16mA
110	0.54V	18mA
111	0.6V	20mA

PWM Control 2 (R3Eh)

Reg. No	R/W	RS	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R3Eh	0	1	0	0	0	0	0	0	0	0	0	0	0	0	FPWM 2	FPWM 1	FPWM 0	DPWM 2	DPWM 1	DPWM 0

FPWM2–0: Control PWM frequency. Default=”010”;

FPWM2–0	PWM frequency
000	1.2M
001	600K
010	300K
011	150K
100	75K
101	37.5K
110	Setting disable
111	

DPWM2–0: Control PWM Drive output clock duty. Default=”110”;

DPWM 2–0	PWM duty
000	0
001	12.5%
010	25%
011	37.5%
100	50%
101	62.5%
110	75%
111	87.5%

FSM Control 3

Reg. No	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R3Fh	0	1	0	0	0	0	0	0	0	0	0	0	0	EFSM	IBZ	CFSM 2	CFSM 1	CFSM 0

CFSM2-0: Adjust FSM clock cycle. Default=”000”

CFSM2-0	FSM clock cycle
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	1

IBZ: Immediately back to zero duty. Default=”1”

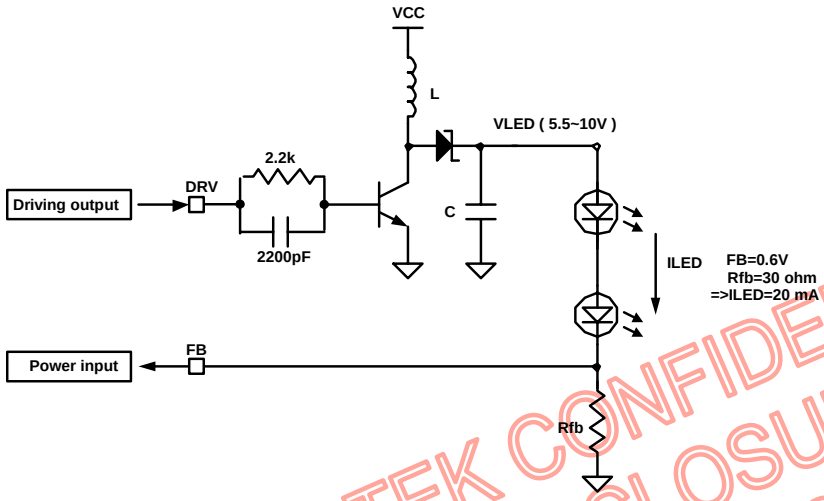
IBZ	Immediately back to zero duty
0	Still
1	Immediately back to zero duty

EFSM: Enable FSM. Default=”1”

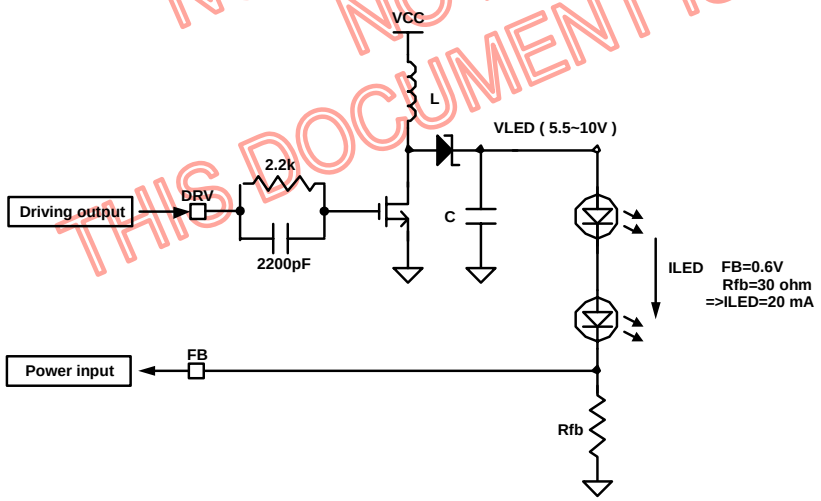
EFSM	FSM output
0	Disable
1	Enable

PWM Application Examples as the following:

PWM Application Circuit 1



PWM Application Circuit 2



*** PWM function setting**

C=2.2uF, L=47uH

Item	Value
VFB	0.6V
FPWM	150K
DPWM	75%
CFSM	8
IBZ	0

RESET FUNCTION

The NT3915 is internally initialized by RESET input. While in reset-procedure, NT3915 is busy, so it cannot accept instructions from MPU or data access from GRAM. The reset input must be held for at least 1 ms. Do not access the GRAM or initially set the instructions until the R-C oscillation frequency is stable after power has been supplied (10 ms).

Instruction Set Initialization

1. Start oscillation executed
2. Driver output control (NL4–0 = 10101, SS = 0, GS = 0)
3. LCD driving AC control (FLD1-0 = 01, B/C = 0, EOR = 0, NW5–0 = 00000)
4. Power control 1 (BT2-0 = 000, DC2–0 = 000, AP2–0 = 000: LCD power off, SLP = 0, STB = 0: Standby mode off)
5. Power control 2 (OPF = 0)
6. Entry mode set (HWM = 0, I/D1-0 = 11: Increment by 1, AM = 0: Horizontal move, LG2–0 = 000: Replace mode, BGR=0)
7. Compare register (CP15–0: 00/0000/0000/0000/0000)
8. Display control 1 (PT1-0 = 00, VLE2–1 = 00: No vertical scroll, SPT = 0, GON = 0, DTE = 0, CL = 0: 260K-color mode, REV = 0, D1–0 = 00: Display off)
9. Frame cycle control (NO1-0 = 00, SDT1-0 = 00, EQ1-0 = 00: no equalization, DIV1-0 = 00: 1-divided clock, RTN3-0 = 0000: 16 clock cycle in 1H period)
10. Power control 3 (VC2-0 = 000)
11. Power control 4 (VRL3-0 = 0000, PON=0, VRH3-0 = 0000)
12. Power control 5 (VCOMG = 0, VDV4-0 = 00000, VCM4-0 = 00000)
13. RAM address set (AD15–0 = 0000h)
14. RAM write data mask (WM15–0 = 0000h: No mask)
15. Gamma control
    (PKP02–00 = 000, PKP12–10 = 000, PKP22–20 = 000, PKP32–30 = 000,
    PK42–40 = 000, PKP52–50 = 000, PRP02–00 = 000, PRP12–10 = 000)
    (PKN02–00 = 000, PKN12–10 = 000, PKN22–20 = 000, PKN32–30 = 000,
    PKN42–40 = 000, PKN52–50 = 000, PRN02–00 = 000, PRN12–10 = 000)
    (VRP03-00 = “0000”, VRP14-10=”00000”, VRN03-00=”0000”, VRN14-10=”00000”)
16. Gate scanning starting position (SCN4-0 = 00000)
17. Vertical scroll (VL7–0 = 0000000)
18. 1st screen division (SE17-10 = 11111111, SS17-10 = 00000000)
19. 2nd screen division (SE27-20 = 11111111, SS27-20 = 00000000)
20. Horizontal RAM address position (HEA7-0 = 10000011, HSA7-0 = 00000000)
21. Vertical RAM address position (VEA7-0 = 10101111, VSA7-0 = 00000000)
22. PWM Control 1 (VFB2–0=000)
23. PWM Control 2 (FPWM2–0=010, DPWM2–0=110)
24. FSM Control 3 (CFSM=0000,IBZ=1,EFSM=1)

GRAM Data Initialization

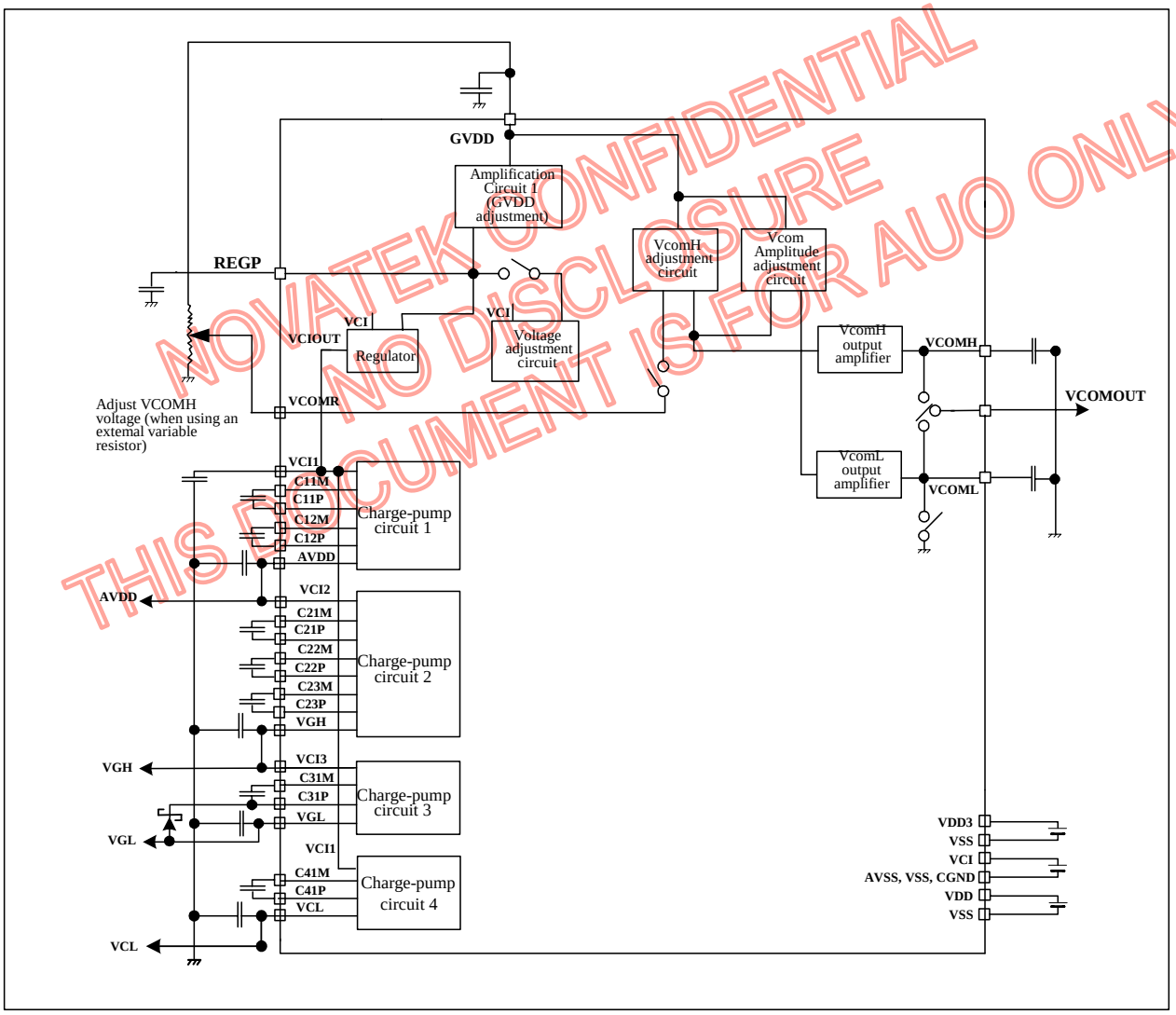
GRAM is not automatically initialized by reset input but must be initialized by software while display is off (D1-0 = 00).

Output Pin Initialization

1. LCD driver output pins (Source output) : Output VSS level
   (Gate output) : Output VGH level
2. Oscillator output pin (OSC2): Outputs oscillation sign

POWER SUPPLY CIRCUIT

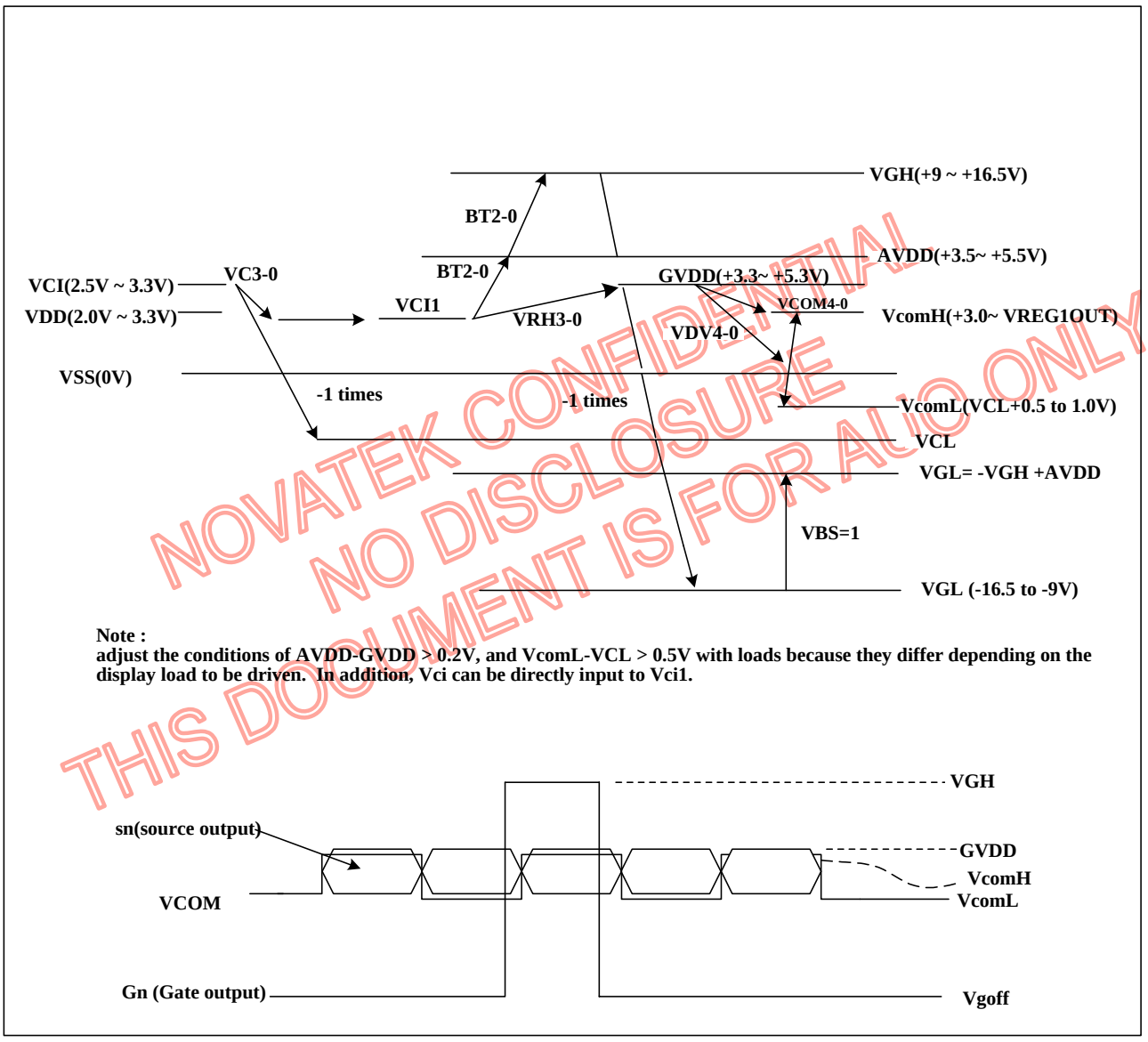
The following figure shows a configuration of the voltage generation circuit for NT3915. The charge-pump circuits consist of charge-pump circuits 1 to 4. Charge-pump circuit1 doubles or triples the voltage supplied to VCI1, and that voltage is doubled, tripled, or quadrupled in charge-pump circuit2. Charge-pump circuit3 reverses the VGH level with reference to VSS or VBS and generates the VGL level. These charge-pump circuits generate power supplies AVDD, GVDD, VGH, VGL, Vgoff, and VCOM. Reference voltages GVDD, VCOM, and Vgoff for the grayscale voltage are amplified in amplification circuits 1 and 2 from the internal-voltage adjustment circuit or the REGP or REGN voltage, and generate each level depending on that voltage. Connect VCOM to the TFT panel.



Configuration of the Internal Power-supply Circuit

PATTERN DIAGRAMS FOR VOLTAGE SETTING

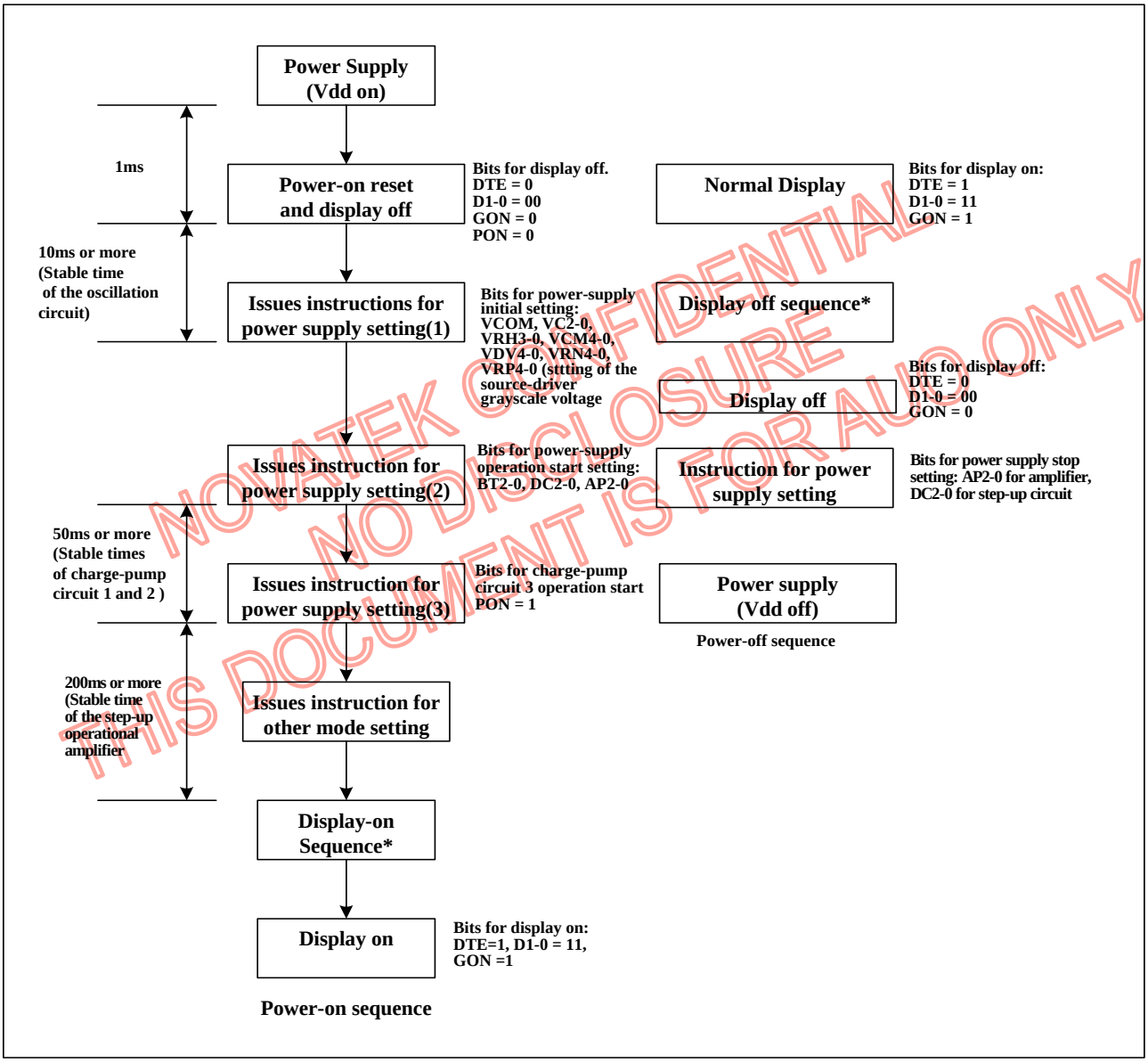
The following figure shows a pattern diagram for the voltage setting and an example of waveforms.



Pattern diagram and an example of waveforms

SET UP FLOW OF POWER SUPPLY

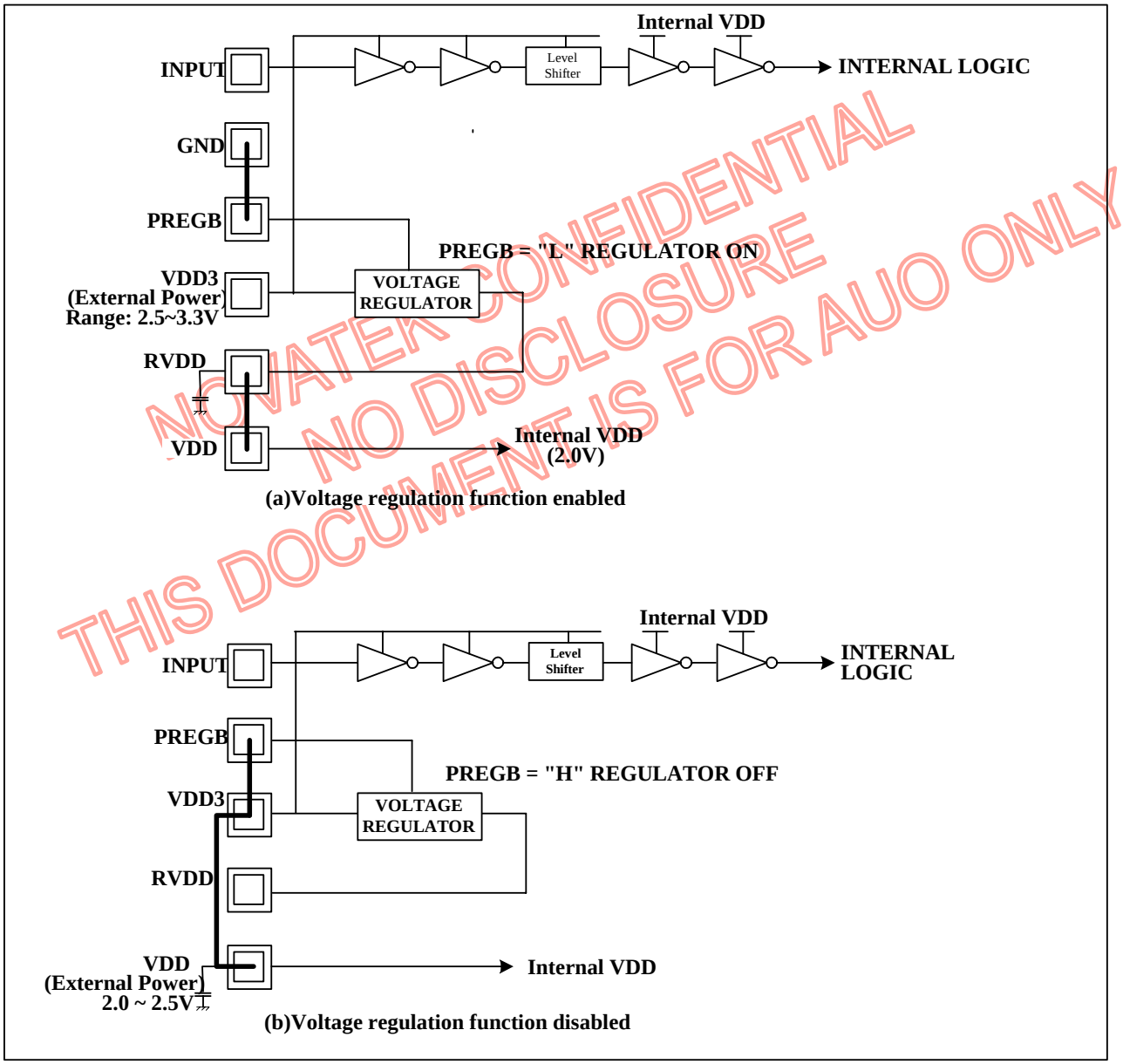
Apply the power in a sequence as shown in the following figure. The stable time of the oscillation circuit, charge-pump circuit, and operational amplifier depend on the external resistor or capacitance.



Set up flow of Power Supply

VOLTAGE REGULATION FUNCTION

The NT3915 have internal voltage regulator. Voltage regulation function is controlled by PregB pin. If PregB= “H”, voltage regulation is stopped. PregB= “L” enables internal voltage regulation function. By use of this function, internal logic circuit damage can be prohibited. Furthermore, power consumption also be obtained. Detailed function description and application setup is described in the following diagram.



Voltage regulation function

SYSTEM INTERFACE

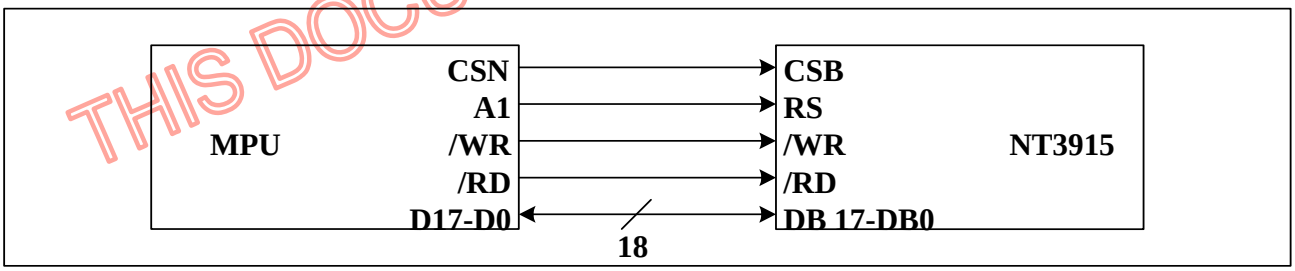
The following interfaces are available as system interface in NT3915. It is determined by setting bits of IM3-0.

IM3- 0	System Interface	DB Pin
0 0 0 0	68-system 16-bit interface	DB17 to10, 8 to1
0 0 0 1	68-system 8-bit interface	DB17 to10
0 0 1 0	80-system 16-bit interface	DB17 to10, 8 to1
0 0 1 1	80-system 8-bit interface	DB17 to10
0 1 0 *	Serial peripheral interface (SPI)	DB1 to 0
0 1 1 *	Setting disabled	-
1 0 0 0	68-system 18-bit interface	DB17 to 0
1 0 0 1	68-system 9-bit interface	DB17 to 9
1 0 1 0	80-system 18-bit interface	DB17 to 0
1 0 1 1	80-system 9-bit interface	DB17 to 9
1 1 * *	Setting disabled	-

Table 10. IM Bits and System Interface

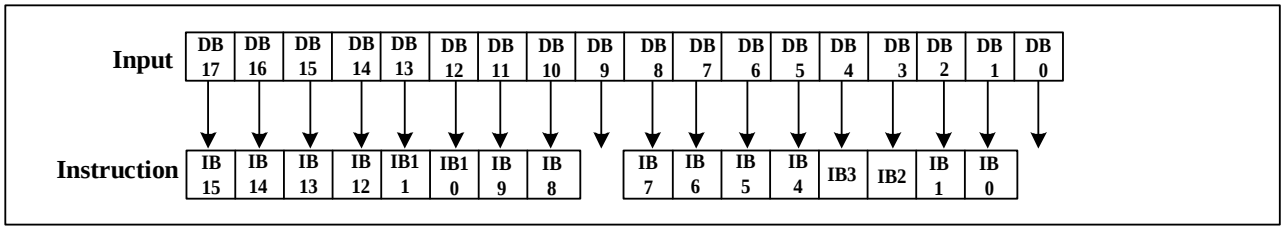
68/80-SYSTEM 18-BIT BUS INTERFACE

Setting the IM3/2/1/0 (interface mode) to the VDD3/VSS/VSS/vSS level allows 68-system 18-bit parallel data transfer. Setting the IM3/2/1/0 to the VDD3/GND/VDD3/GND level allows 80-system 18-bit parallel data transfer.

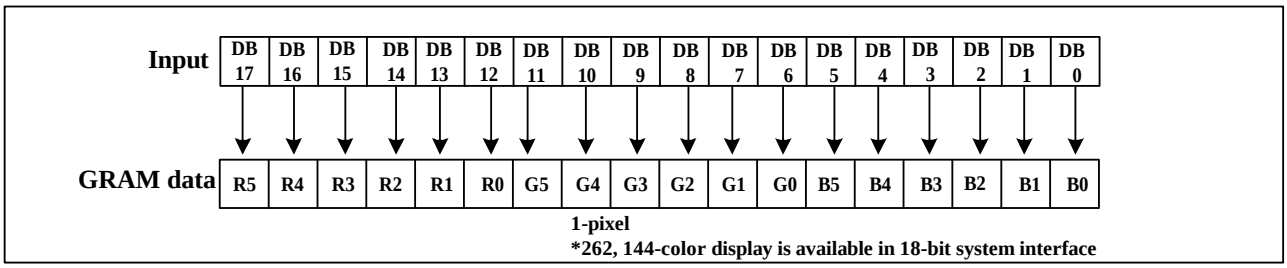


Interface with the 18-bit Microcomputer

68/80 -SYSTEM 18-bit interface data FORMAT



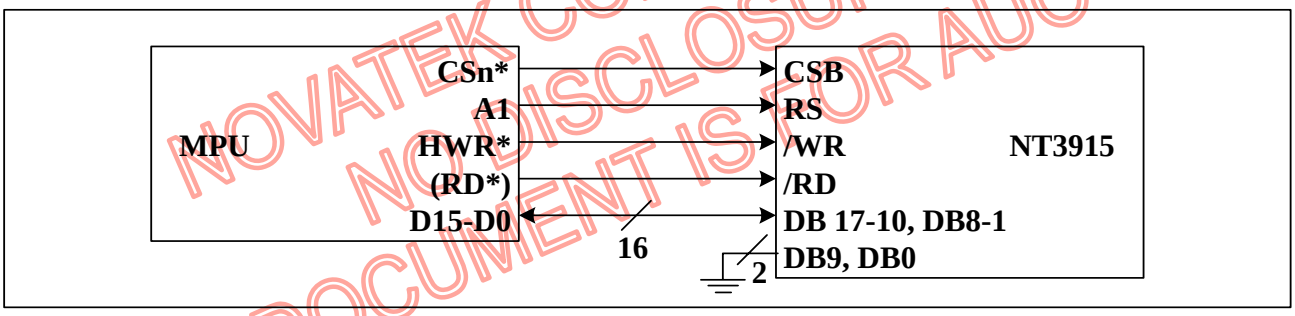
Instruction format for 18-bit Interface



RAM Data write format for 18-bit interface

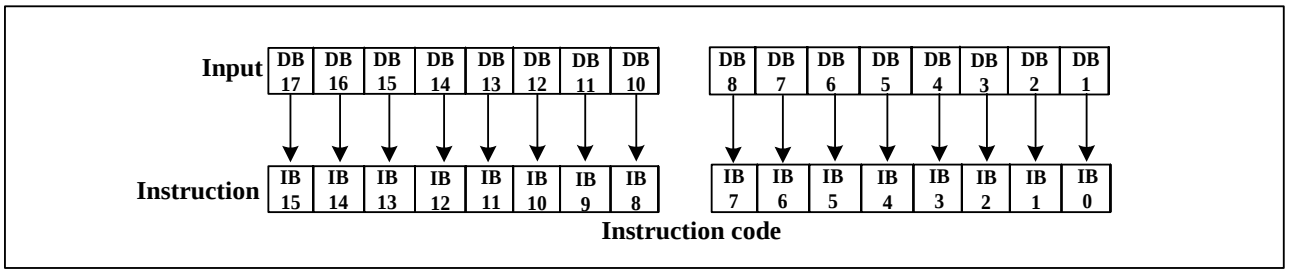
68/80-SYSTEM 16-BIT BUS INTERFACE

Setting the IM3/2/1/0 (interface mode) to the VSS/VSS/VSS/VSS level allows 68-system 16-bit parallel data transfer. Setting the IM3/2/1/0 to the VSS/VSS/VDD3/VSS level allows 80-system 16-bit parallel data transfer.

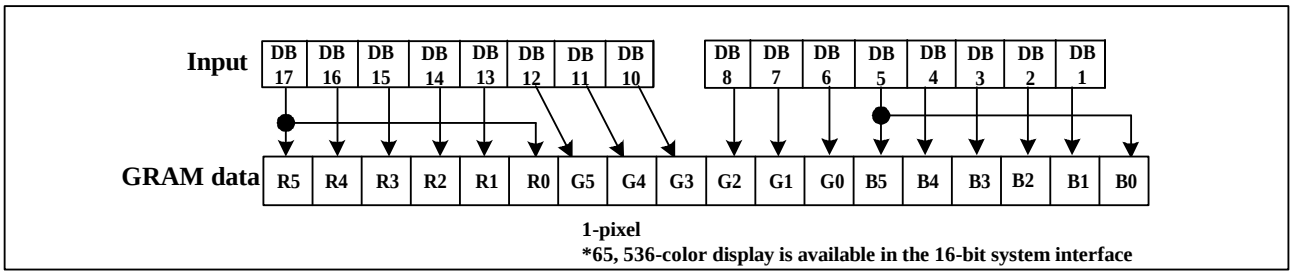


Interface with the 16-bit Microcomputer

68/80 -SYSTEM 16-bit interface data FORMAT



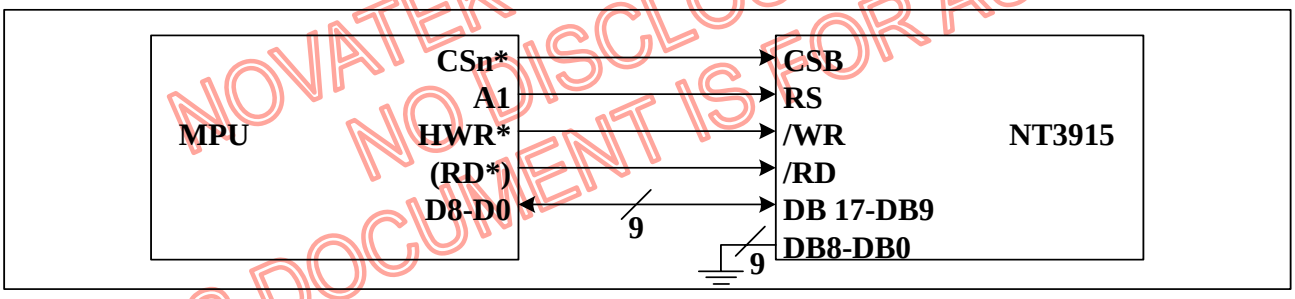
Instruction format for 16-bit Interface



RAM Data write format for 16-bit Interface

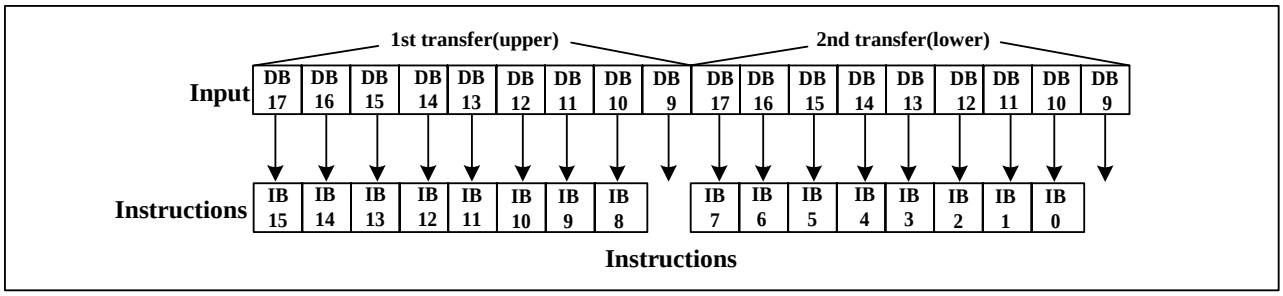
68/80-SYSTEM 9-BIT BUS INTERFACE

Setting the IM3/2/1/0 (interface mode) to the VDD3/VSS/VSS/VDD3 level allows 68-system 9-bit parallel data transfer using pins DB17–DB9. Setting the IM3/2/1/0 to be VDD3/VSS/VDD3/VDD3 level allows 80-system 9-bit parallel data transfer. The 16-bit instructions and RAM data are divided into nine upper/lower bits and the transfer starts from the upper nine bits. Fix unused pins DB8–DB0 to the VDD 3 or VSS level. Note that the upper bytes must also be written when the index register is written.

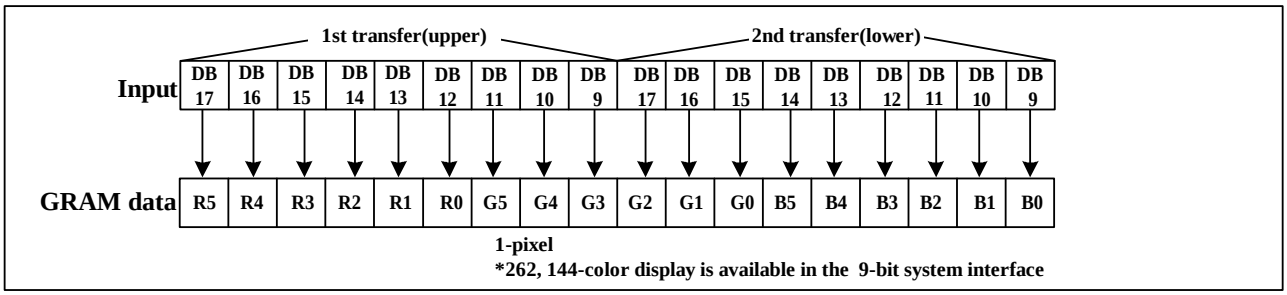


Interface to 9-bit Microcomputer

68/80 -SYSTEM 9-bit interface data FORMAT



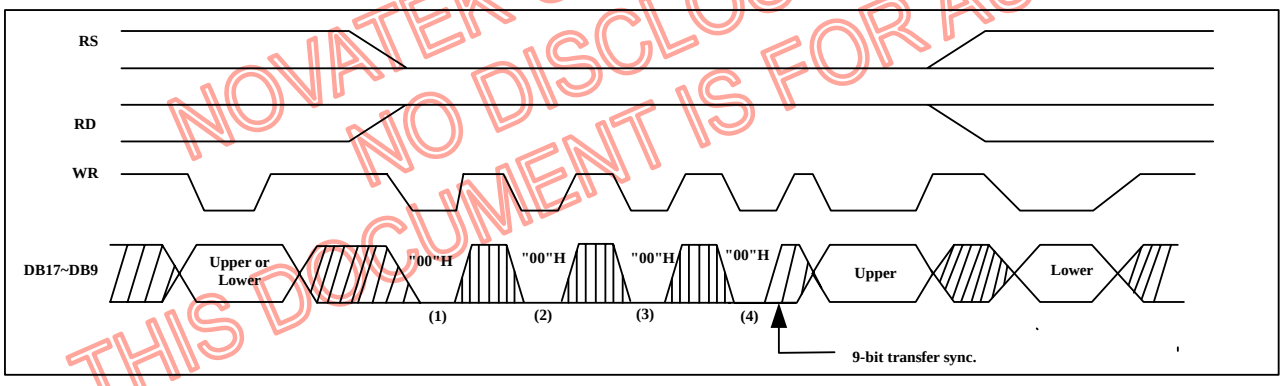
Instruction format for 9-bit Interface



RAM Data write format for 9-bit interface

NOTE: Transfer synchronization function for a 9-bit bus interface

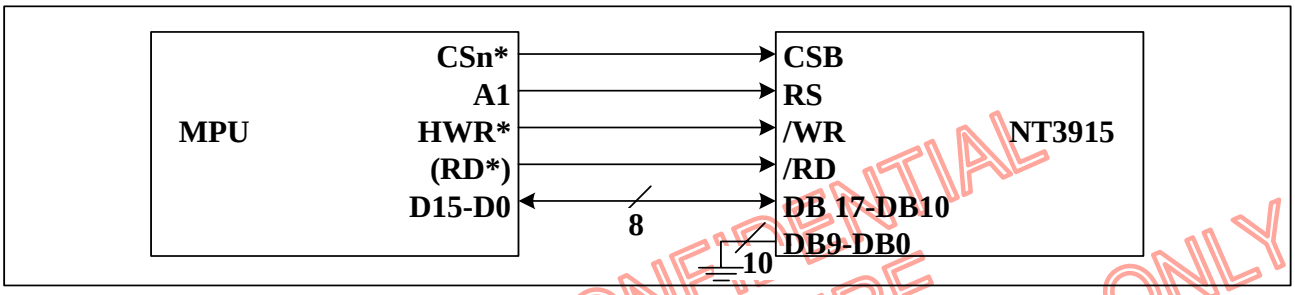
The NT3915 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 9-bit data transfer in the 9-bit bus interface. Noise causing transfer mismatch between the nine upper and lower bits can be corrected by a reset triggered by consecutively writing a “00”H instruction four times. The next transfer starts from the upper nine bits. Executing synchronization function periodically can recover any runaway in the display system.



9-bit Transfer Synchronization

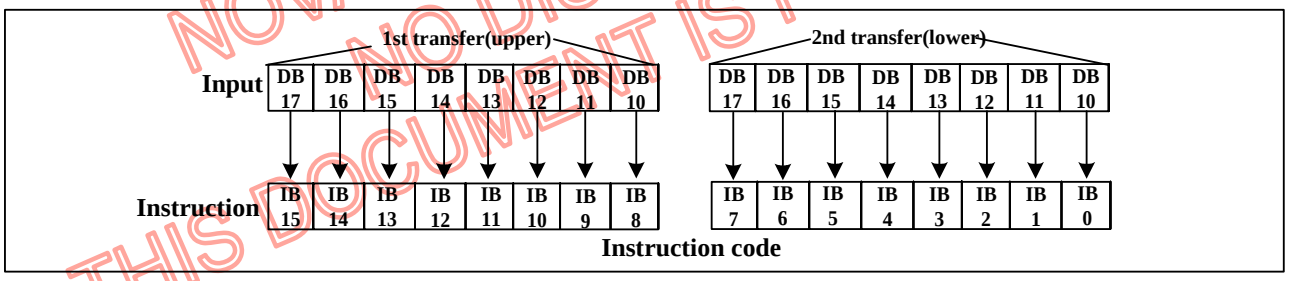
68/80-SYSTEM 8-BIT BUS INTERFACE

Setting the IM3/2/1/0 (interface mode) to the VSS/VSS/VSS/VDD3 level allows 68-system 8-bit parallel data transfer. Setting the IM3/2/1/0 to the VSS/VSS/VDD3/VDD3 level allows 80-system 8-bit parallel data transfer. The 16-bit instructions and RAM data are divided into eight upper/lower bits and the transfer starts from the upper eight bits. Fix unused pins DB9–DB0 to the VDD3 or VSS level. Note that the upper bytes must also be written when the index register is written.

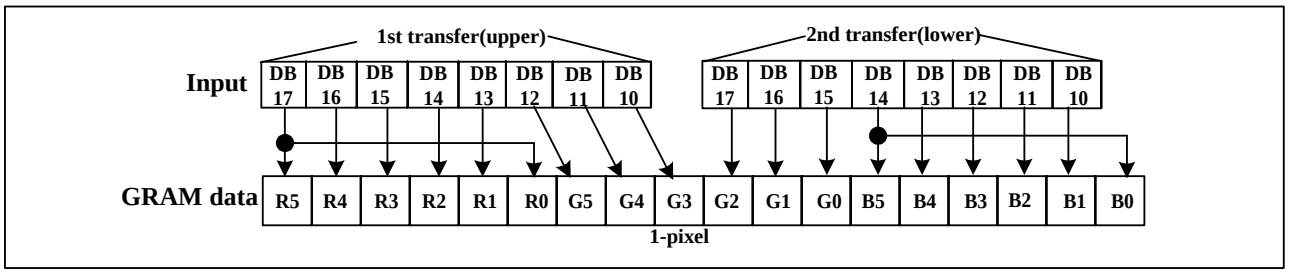


Interface with the 8-bit Microcomputer

68/80 -SYSTEM 8-bit interface data FORMAT



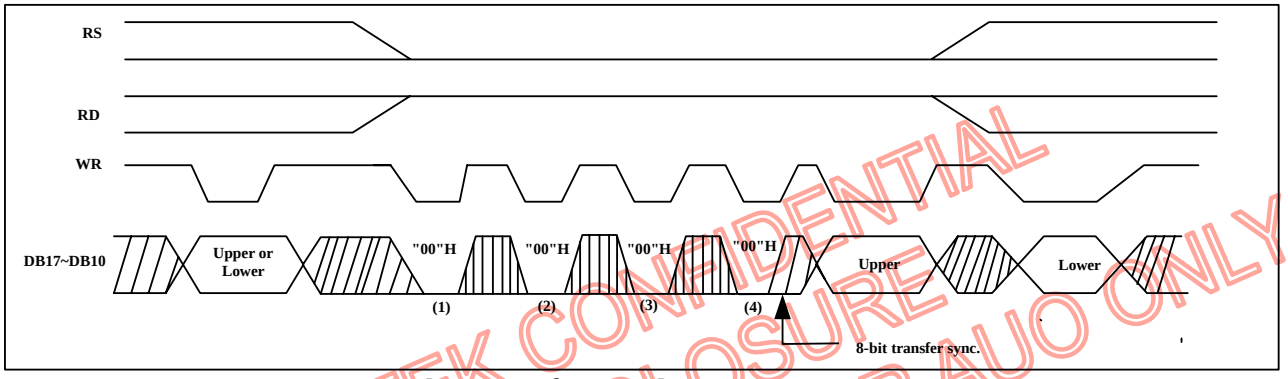
Instruction format for 8-bit Interface



RAM Data write format for 8-bit Interface

NOTE: Transfer synchronization function for an 8-bit bus interface

The NT3915 supports the transfer synchronization function, which resets the upper/lower counter to count upper/lower 8-bit data transfer in the 8-bit bus interface. Noise causing transfer mismatch between the eight upper and lower bits can be corrected by a reset triggered by consecutively writing a “00”H instruction four times. The next transfer starts from the upper eight bits. Executing synchronization function periodically can recover any runaway in the display system



8-bit Transfer Synchronization

SERIAL DATA TRANSFER (SPI)

Setting the IM3 pin to the VSS level allows serial peripheral interface (SPI) transfer, using the chip select line (CS*), serial transfer clock line (SCL), serial input data (SDI), and serial output data (SDO). For a serial interface, the IM0/ID pin function uses an ID pin. If the chip is set up for serial interface, the DB17-2 pins that are not used must be fixed at VDD3 or VSS.
The NT3915 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.
The NT3915 is selected when the 6-bit chip address in the start byte matches the 6-bit device identification code that is assigned to the NT3915. When selected, the NT3915 receives the subsequent data string. The LSB of the identification code can be determined by the ID pin. The five upper bits must be 01110. Two different chip addresses must be assigned to a single NT3915 because the seventh bit of the start byte is used as a register select bit (RS): that is, when RS = 0, data can be written to the index register or status can be read, and when RS = 1, an instruction can be issued or data can be written to or read from RAM. Read or write is selected according to the eighth bit of the start byte (R/W bit). The data is received when the R/W bit is 0, and is transmitted when the R/W bit is 1.
After receiving the start byte, the NT3915 receives or transmits the subsequent data byte-by-byte. The data is transferred with the MSB first. All NT3915 instructions are 16 bits. Two bytes are received with the MSB first (DB17 to 0), then the instructions are internally executed. After the start byte has been received, the first byte is fetched as the upper eight bits of the instruction and the second byte is fetched as the lower eight bits of the instruction.
Four bytes of RAM read data after the start byte are invalid. The NT3915 starts to read correct RAM data from the fifth byte.

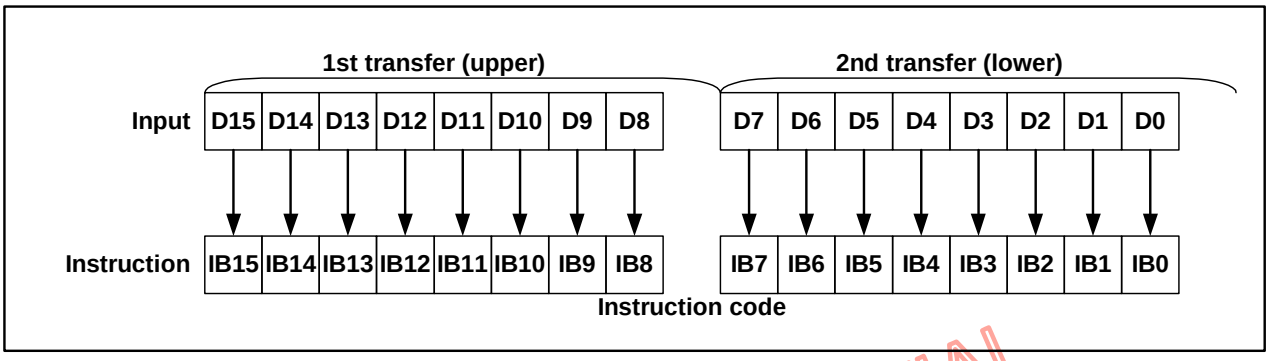
Transfer bit	S	1	2	3	4	5	6	7	8
Start byte format	Transfer start	Device ID code						RS	R/W
		0	1	1	1	0	ID	*	*

Table 11. Start Byte Format

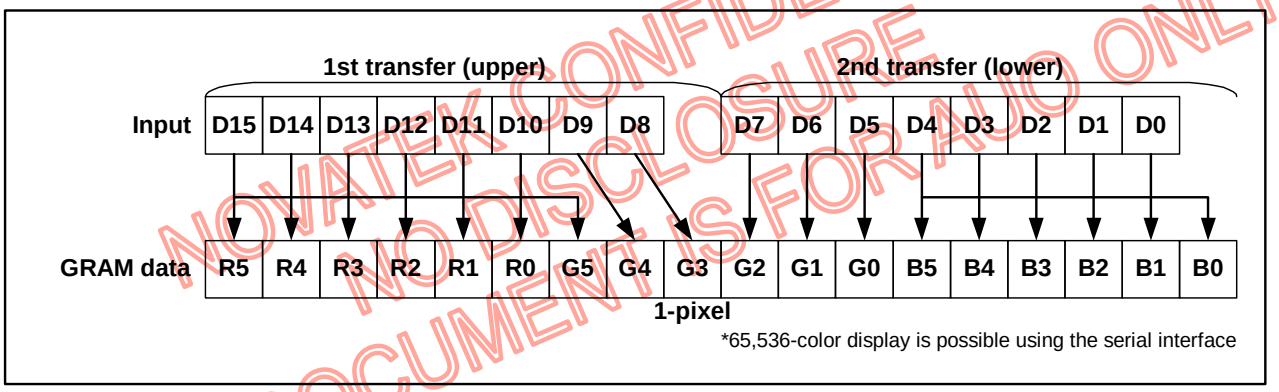
NOTE: ID bit is selected by the IM0/ID pin.

RS	RW	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or RAM data
1	1	Reads instruction or RAM data

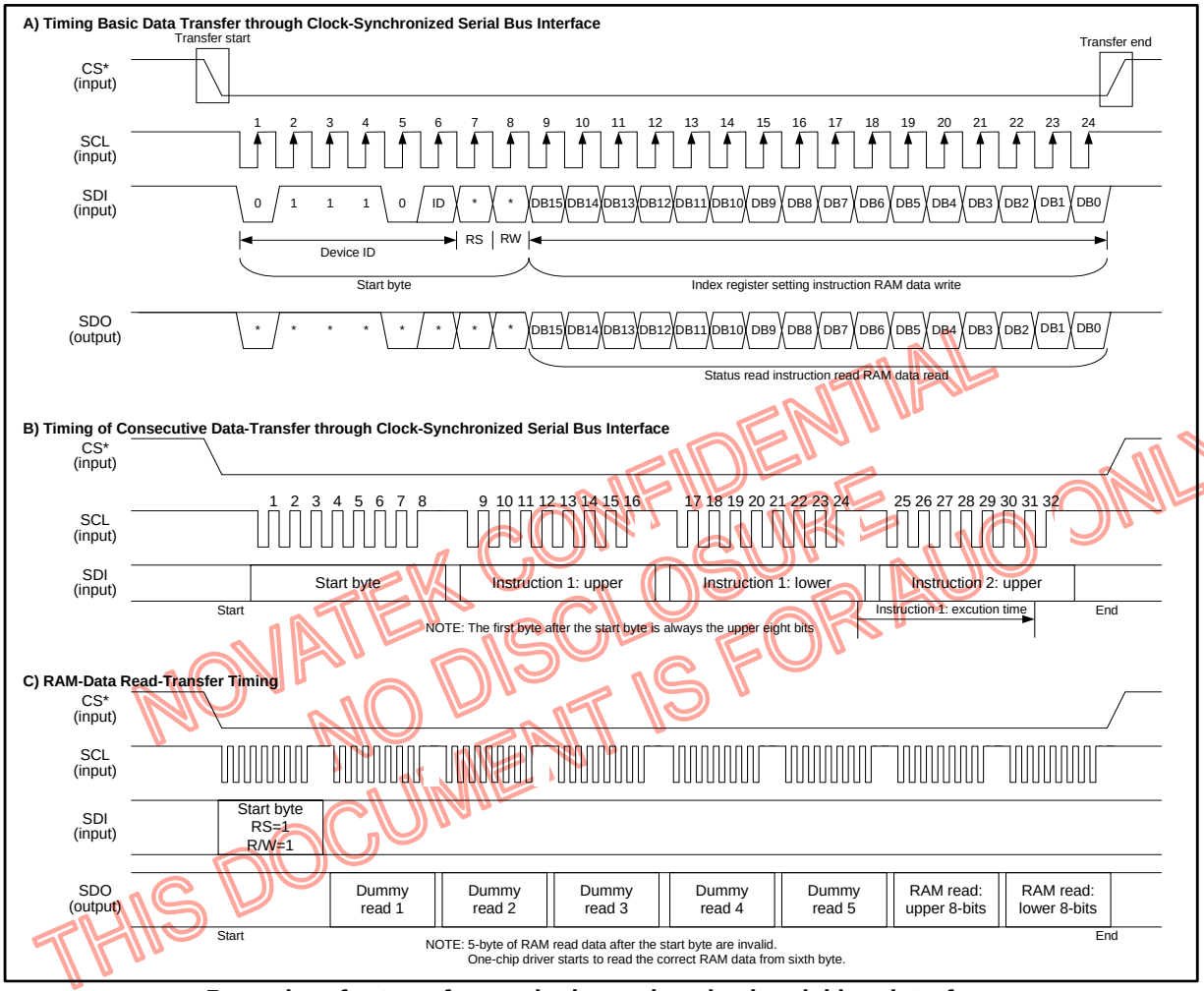
Table 12. RS and R/W Bit Function



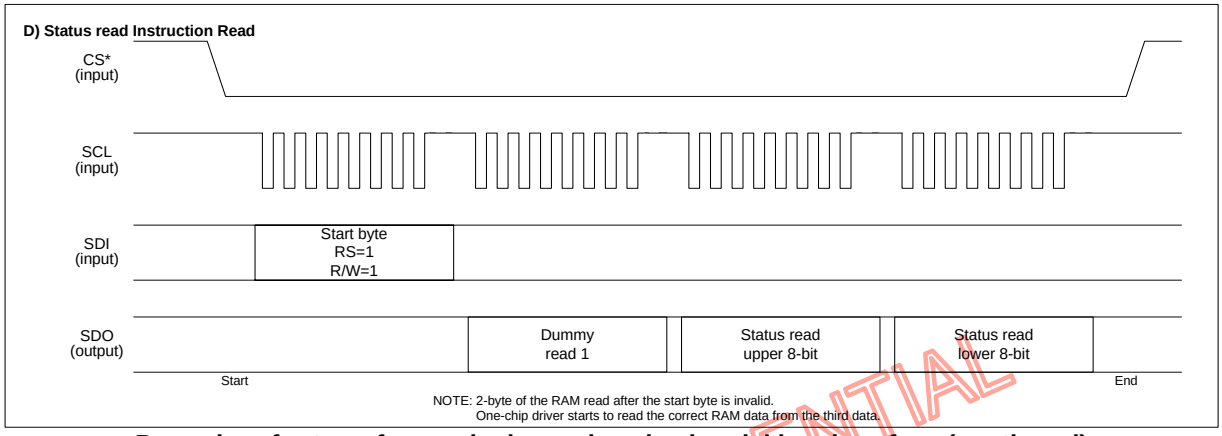
Instruction format for Serial Data Transfer



RAM Data Write format for Serial Data Transfer



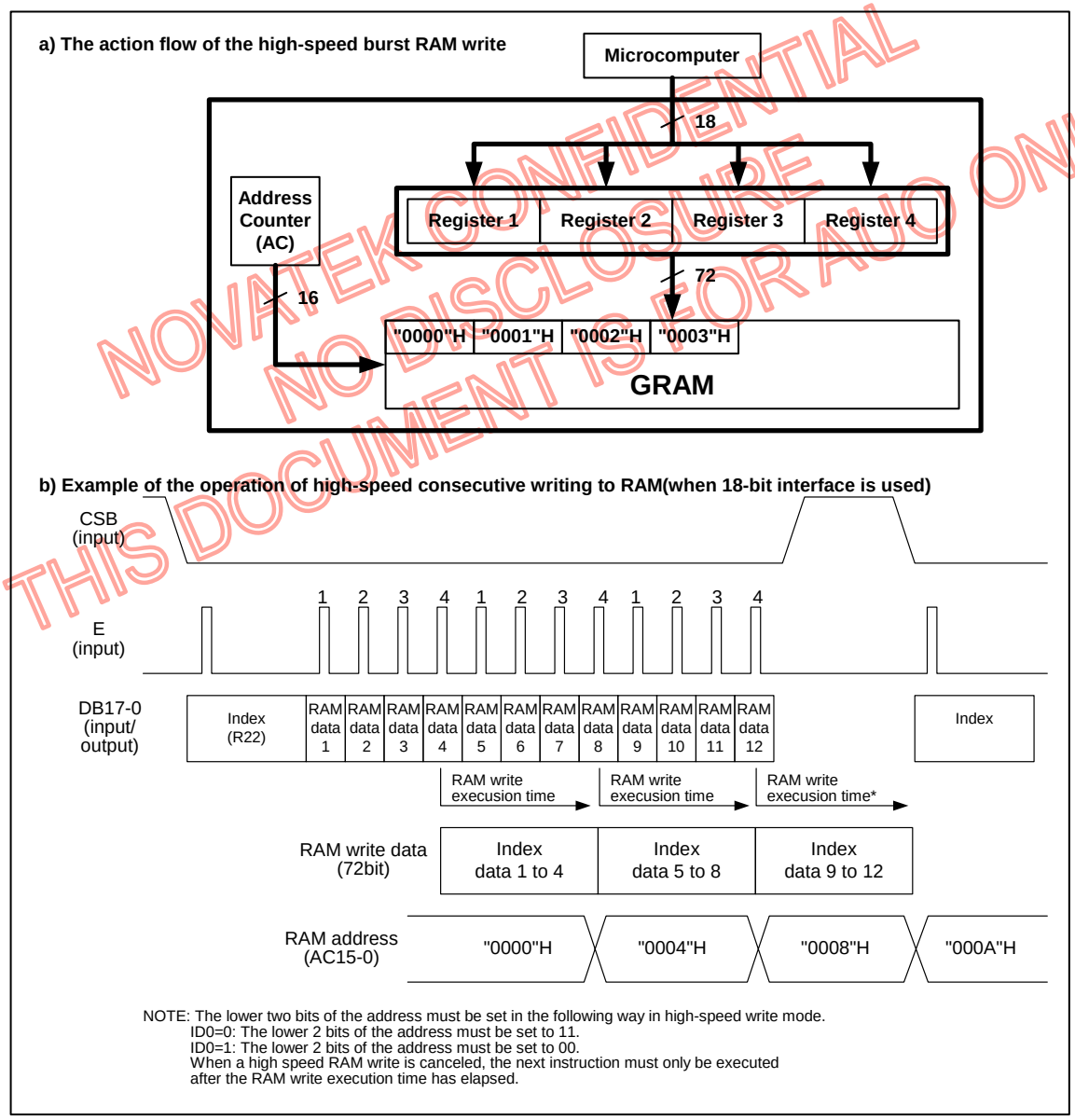
Procedure for transfer on clock synchronized serial bus interface



Procedure for transfer on clock synchronized serial bus interface (continued)

HIGH-SPEED BURST RAM WRITE FUNCTION

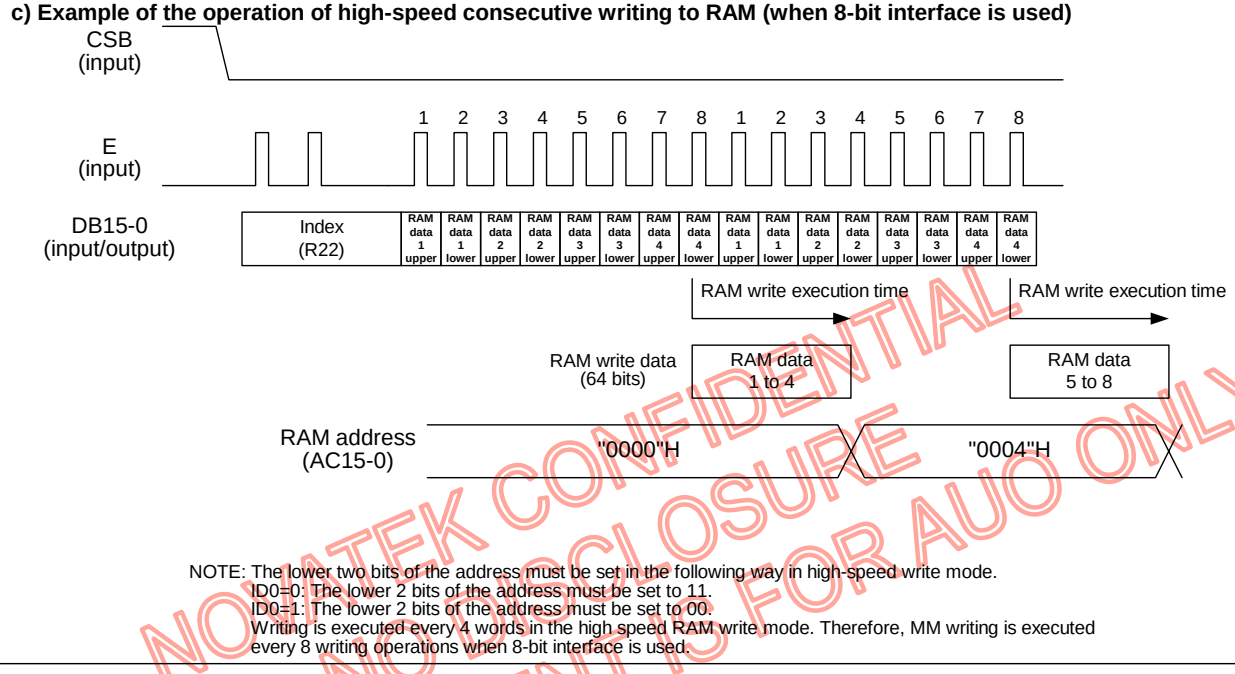
The NT3915 has a high-speed burst RAM-write function that can be used to write data to RAM in one-fourth the access time required for an equivalent standard RAM-write operation. This function is especially suitable for applications that require the high-speed rewriting of the display data, for example, display of color animations, etc.
When the high-speed RAM-write mode (HWM) is selected, data for writing to RAM is once stored to the NT3915 internal register. When data is selected four times per word, all data is written to the on-chip RAM. While this is taking place, the next data can be written to an internal register so that high-speed and consecutive RAM writing can be executed for animated displays, etc.



NOTE: The lower two bits of the address must be set in the following way in high-speed write mode.
ID0=0: The lower 2 bits of the address must be set to 11.
ID0=1: The lower 2 bits of the address must be set to 00.
When a high speed RAM write is canceled, the next instruction must only be executed after the RAM write execution time has elapsed.

Example of the operation of high-speed consecutive writing to RAM

c) Example of the operation of high-speed consecutive writing to RAM (when 8-bit interface is used)



NOTE: The lower two bits of the address must be set in the following way in high-speed write mode.
ID0=0: The lower 2 bits of the address must be set to 11.
ID0=1: The lower 2 bits of the address must be set to 00.
Writing is executed every 4 words in the high speed RAM write mode. Therefore, MM writing is executed every 8 writing operations when 8-bit interface is used.

Example of the operation of high-speed consecutive writing to RAM (8-bit interface)

When high-speed write mode is used, note the following.

1. The logical and compare operations cannot be used.
2. Data is written to RAM each four words. When an address is set, the lower two bits in the address must be set to the following values.
*When ID0=0, the lower two bits in the address must be set to 11 and be written to RAM.
*When ID0=1, the lower two bits in the address must be set to 00 and be written to RAM.
3. Data is written to RAM each four words. If less than four words of data is written to RAM, the last data will not be written to RAM.
4. When the index register and RAM data write (R22h) have been selected, the data is always written first. RAM cannot be written to and read from at the same time. HWM must be set to 0 while RAM is being read.
5. High-speed and normal RAM write operations cannot be executed at the same time. The mode must be switched and the address must then be set.
6. When high-speed RAM write is used with a window address-range specified, dummy write operation may be required to suit the window address range-specification. Refer to the High-Speed RAM Write in the Window Address section.

	Normal RAM Write (HWM=0)	High-speed RAM Write (HWM=1)
Logical operation function	Can be used	Cannot be used
Compare operation function	Can be used	Cannot be used
BGR function (RGB swap)	Can be used	Can be used
Write mask function	Can be used	Can be used
RAM address set	Can be specified by word	ID0 bit=0: Set the lower two bits to 11 ID0 bit=1: Set the lower two bits to 00
RAM read	Can be read by word	Cannot be used
RAM write	Can be written by word	Dummy write operations may have to be inserted according to a window address-range specification
Window address	Can be set by word	The horizontal range(HAS/HSE): More than four words The number of horizontal writing: 4N(N>2)
External display interface	Can be used	Can be used
AM setting	AM=1/0	AM=0

Table 13. Comparison between Normal and High-speed RAM Write Operations

NOTE: 1 word = 2 byte.

HIGH-SPEED RAM WRITE IN THE WINDOW ADDRESS

When a window address range is specified, GRAM data that is in an optional window area can be updated quickly and continuously by use of dummy write operation. So that the number of RAM access become 4N as shown in the table below.
Dummy write operation must be inserted at the first or last of a row of data, depending on the horizontal window-address range specification bits (HSA1 to 0, HEA1 to 0). Numbers of dummy write operations of a row must be 4N.

HSA1	HSA0	Number of dummy write operations to be inserted at the start of a row
0	0	0
0	1	1
1	0	2
1	1	3

Table 13. Number of Dummy Write Operations in High-Speed RAM Write (HSA bits)

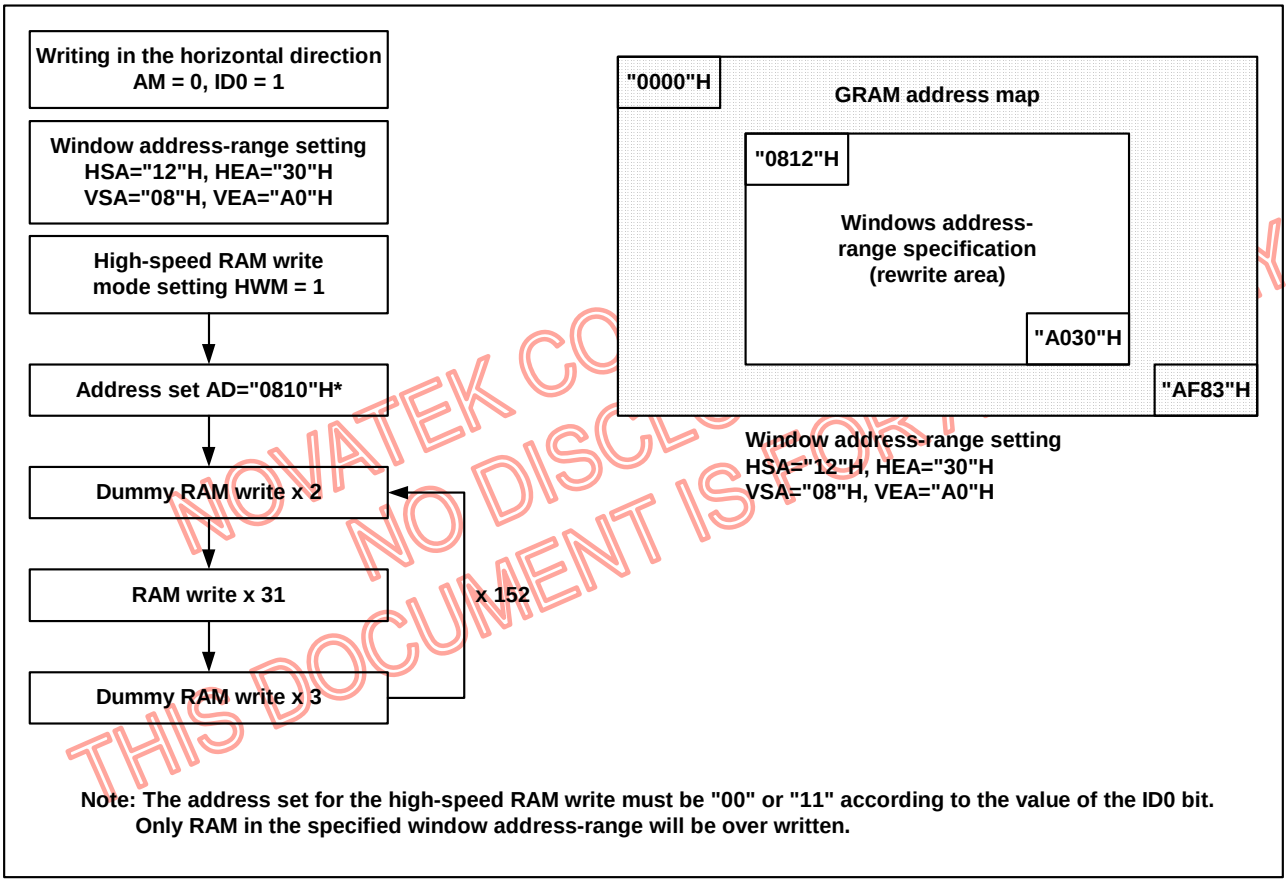
HEA1	HEA0	Number of dummy write operations to be inserted at the end of a row
0	0	3
0	1	2
1	0	1
1	1	0

Table 14. Table 29. Number of Dummy Write Operations in High-Speed RAM Write (HEA bits)

NOTE: Each row of access must consist of 4 X N operations, including the dummy writes.
Horizontal access count = first dummy write count + write data count + last dummy write count = 4 X N

An example of high-speed RAM write with a window address-range specified is shown below.

The window address-range can be accessed consecutively and quickly by inserting two dummy writes at the start of a row and three dummy writes at the end of a row, as determined by using the window address-range specification bits (HSA1 to 0=10, HEA1 to 0=00).

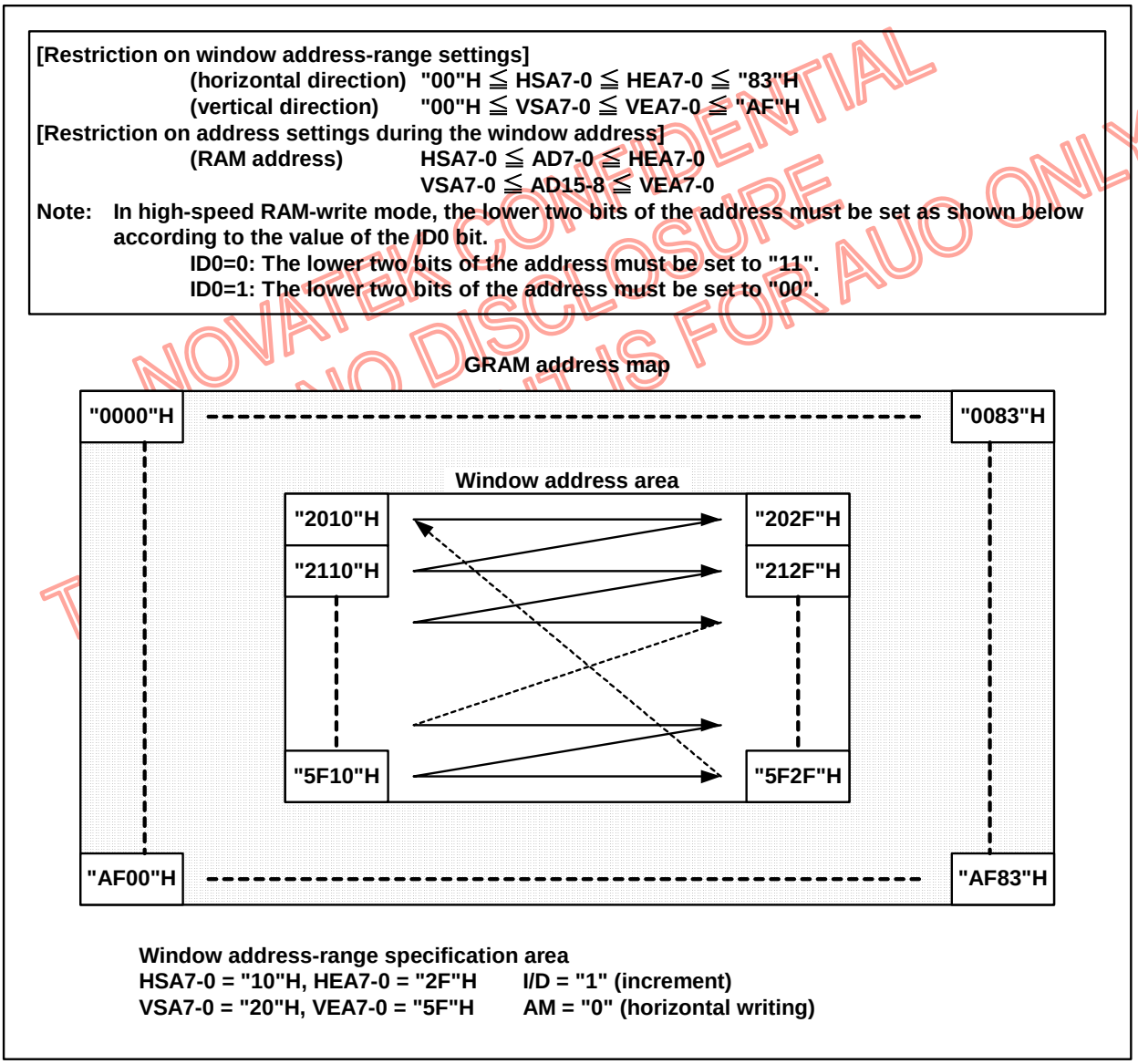


Example of High-speed RAM Write with a window address-range specification

WINDOW ADDRESS FUNCTION

When data is written to the on-chip GRAM, a window address-range which is specified by the horizontal address register (start: HSA7-0, end: HEA 7-0) and vertical address register (start: VSA7-0, end: VEA7-0) can be updated consecutively.
Data is written to addresses in the direction specified by the AM and ID1-0bit. When image data, etc. is being written, data can be written consecutively without thinking a data wrap by doing this.
The window must be specified to be within the GRAM address area described as following example. Addresses must be set within the window address.

[Restriction on window address-range settings]
(horizontal direction) "00"H ≦ HSA7-0 ≦ HEA7-0 ≦ "83"H
(vertical direction) "00"H ≦ VSA7-0 ≦ VEA7-0 ≦ "AF"H
[Restriction on address settings during the window address]
(RAM address) HSA7-0 ≦ AD7-0 ≦ HEA7-0
VSA7-0 ≦ AD15-8 ≦ VEA7-0
Note: In high-speed RAM-write mode, the lower two bits of the address must be set as shown below according to the value of the ID0 bit.
ID0=0: The lower two bits of the address must be set to "11".
ID0=1: The lower two bits of the address must be set to "00".



Example of address operation in the window address specification

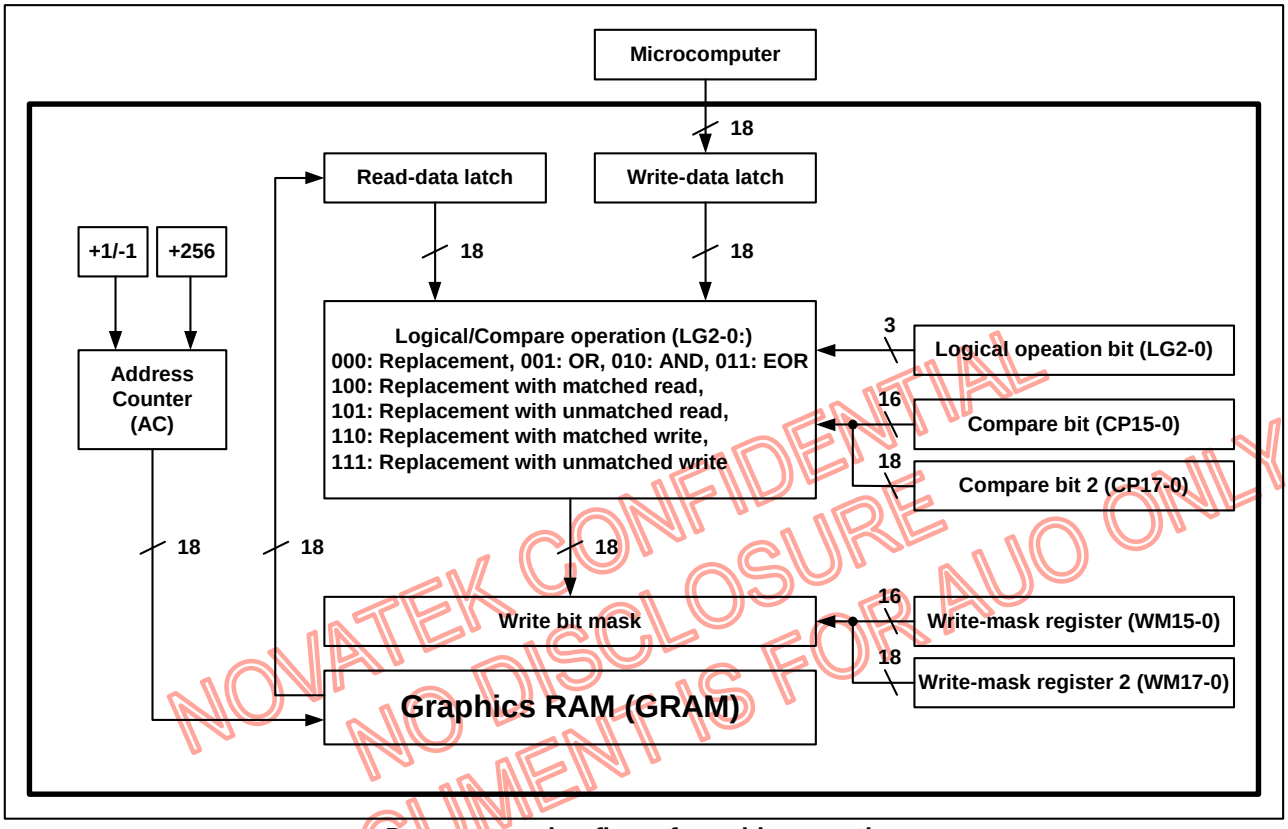
GRAPHICS OPERATION FUNCTION

The NT3915 can greatly reduce the load of the microcomputer graphics software processing through the 16-bit bus architecture and internal graphics-bit operation function. This function supports the following:

1. A write data mask function that selectively rewrites some of the bits in the 18-bit write data.
2. A logical operation write function that writes the data sent from the microcomputer and the original RAM data by a logical operation.
3. A conditional write function that compares the original RAM data or write data and the compare-bit data and writes the data sent from the microcomputer only when the conditions match. Even if the display size is large, the display data in the graphics RAM (GRAM) can be quickly rewritten. The graphics bit operation can be controlled by combining the entry mode register, the bit set value of the RAM-write-data mask register, and the read/write from the microcomputer.

Operation mode	Bit setting			Operation and usage
	I/D	AM	LG2-0	
Write mode 1	0/1	0	000	Horizontal data replacement, horizontal-border drawing
Write mode 2	0/1	1	000	Vertical data replacement, vertical-border drawing
Write mode 3	0/1	0	110 111	Conditional horizontal data replacement, horizontal -border drawing
Write mode 4	0/1	1	110 111	Conditional vertical data replacement, vertical-border drawing
Read/write mode 1	0/1	0	001 010 011	Horizontal data write with logical operation, horizontal -border drawing
Read/write mode 2	0/1	1	001 010 011	Vertical data write with logical operation, vertical-border drawing
Read/write mode 3	0/1	0	100 101	Conditional horizontal data replacement, horizontal -border drawing
Read/write mode 4	0/1	1	100 101	Conditional vertical data replacement, vertical-border drawing

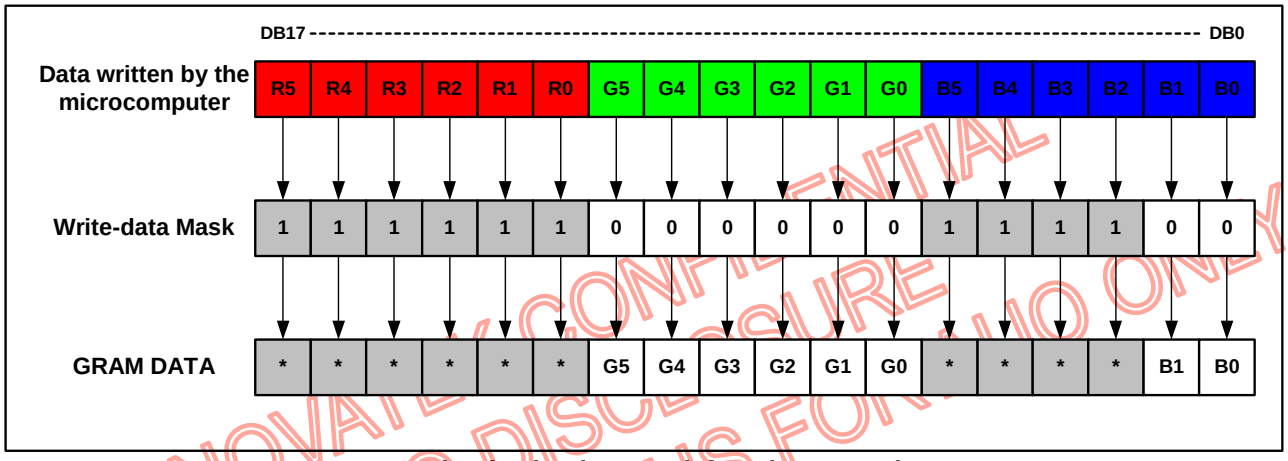
Table 15. Graphics Operation



Data processing flow of graphic operation

WRITE-DATA MASK FUNCTION

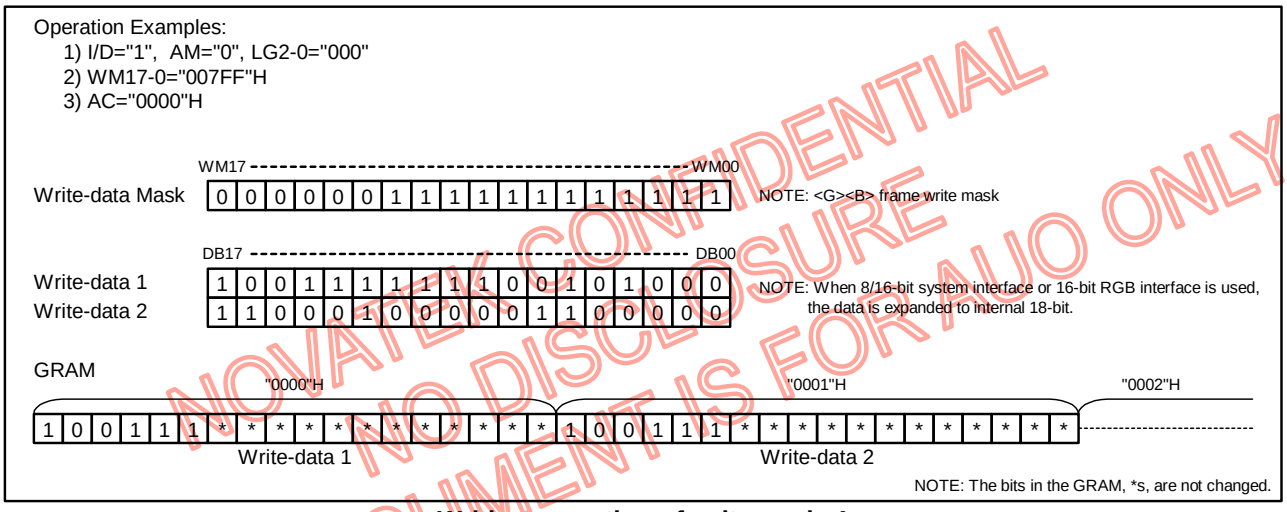
The NT3915 has a bit-wise write-data mask function that controls writing the two-byte data from the microcomputer to the GRAM. Bits that are 0 in the write-data mask register (WM17–0 or WM15-0) cause the corresponding DB bit to be written to the GRAM. Bits that are 1 prevent writing to the corresponding GRAM bit to the GRAM; the data in the GRAM is maintained. This function can be used when only one-pixel data is rewritten or the particular display color is selectively rewritten.



Example of write-data mask function operation

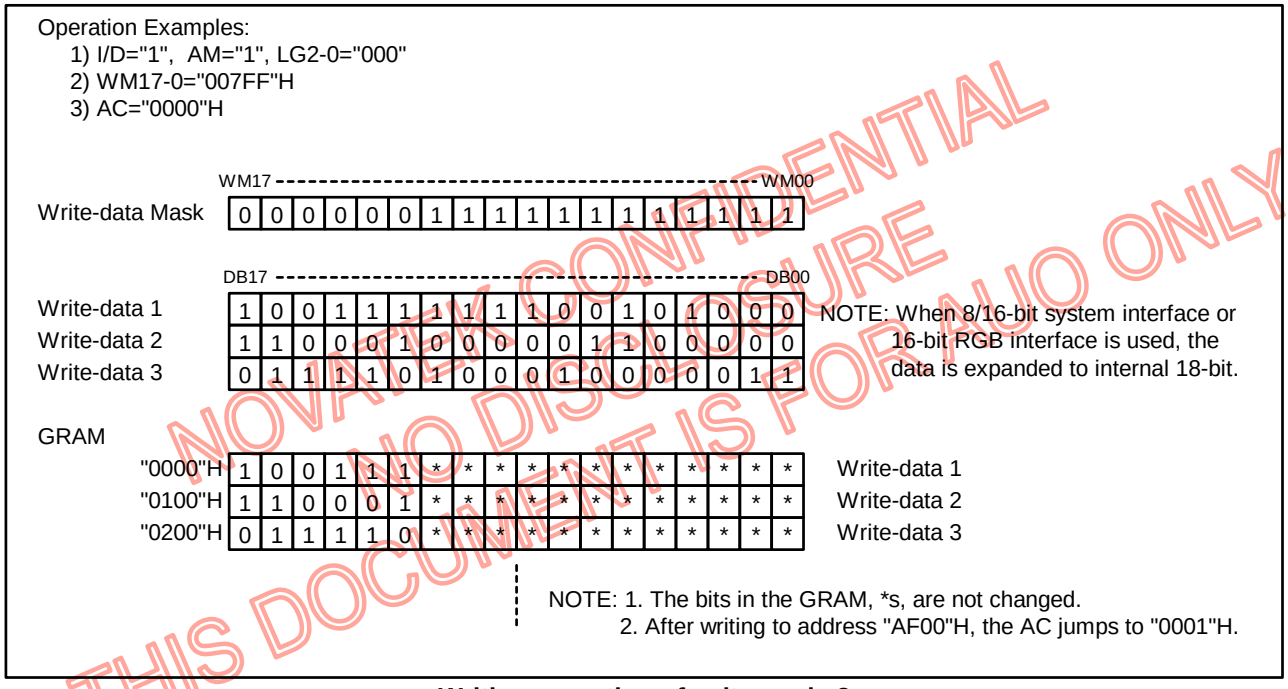
GRAPHICS OPERATION PROCESSING

1. Write mode 1: AM = 0, LG2–0 = 000
   This mode is used when the data is horizontally written at high speed. It can also be used to initialize the graphics RAM (GRAM) or to draw borders. The write-data mask function (WM17–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.



Writing operation of write mode 1

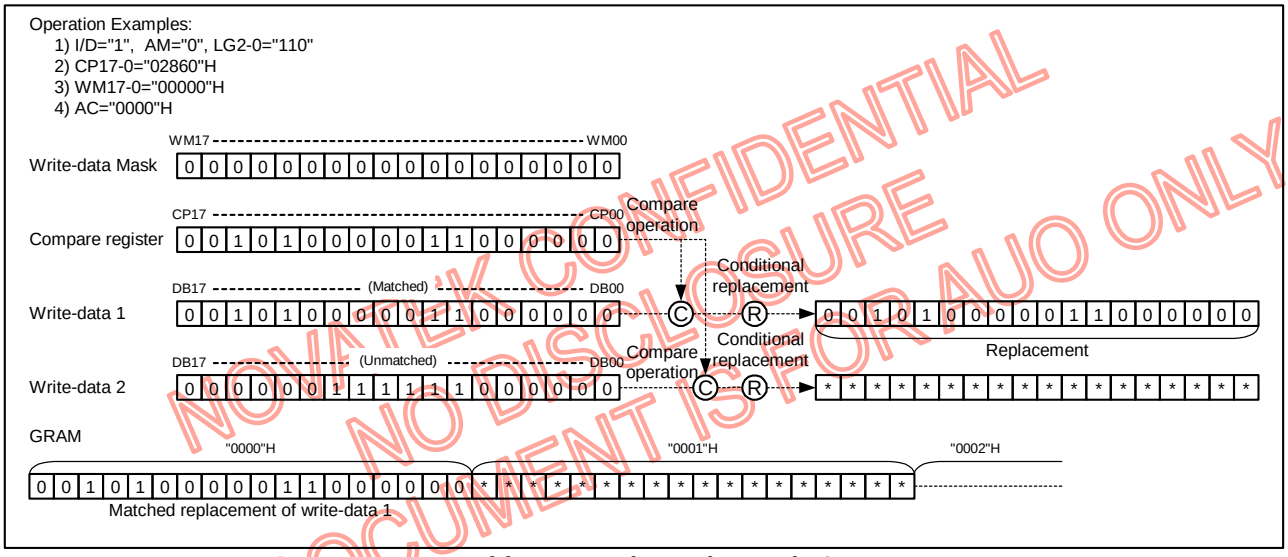
2. Write mode 2: AM = 1, LG2-0 = 000
   This mode is used when the data is vertically written at high speed. It can also be used to initialize the GRAM, develop the font pattern in the vertical direction, or draw borders. The write-data mask function (WM17–0) is also enabled in these operations. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) following the I/D bit after it has reached the lower edge of the GRAM.



Writing operation of write mode 2

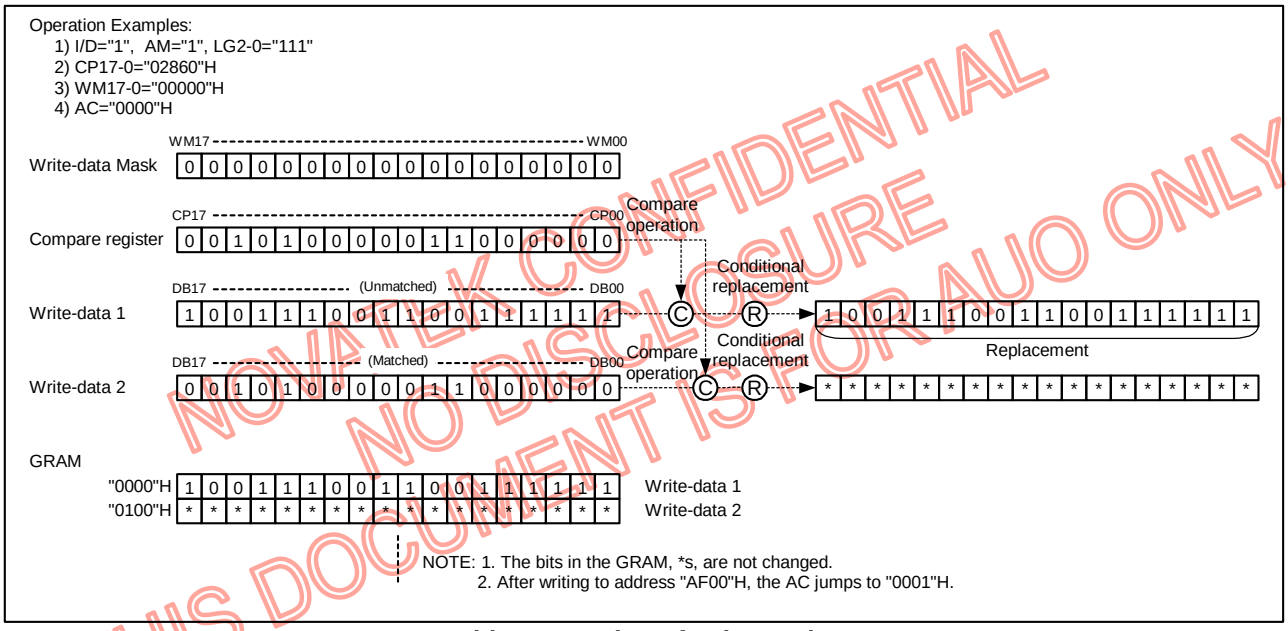
3. Write mode 3: AM = 0, LG2-0 = 110/111

This mode is used when the data is horizontally written by comparing the write data and the set value of the compare register (CP17–0). When the result of the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM15–0) is also enabled. After writing, the address counter (AC) automatically increments by 1 (I/D = 1) or decrements by 1 (I/D = 0), and automatically jumps to the counter edge one-raster-row below after it has reached the left or right edge of the GRAM.



Writing operation write mode 3

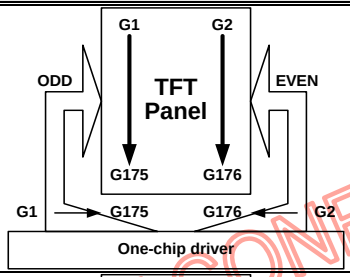
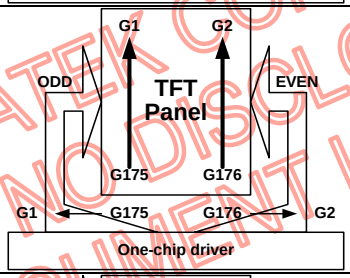
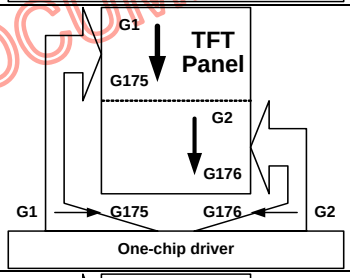
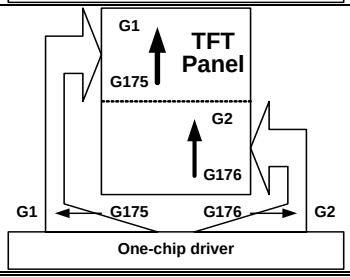
4. Write mode 4: AM =1, LG2-0 = 110/111
   This mode is used when a vertical comparison is performed between the write data and the set value of the compare register (CP17–0) to write the data. When the result by the comparison in a byte unit satisfies the condition, the write data sent from the microcomputer is written to the GRAM. In this operation, the write-data mask function (WM17–0) are also enabled. After writing, the address counter (AC) automatically increments by 256, and automatically jumps to the upper-right edge (I/D = 1) or upper-left edge (I/D = 0) after it has reached the lower edge of the GRAM.



Writing operation of write mode 4

GATE DRIVER SCAN MODE SETTING

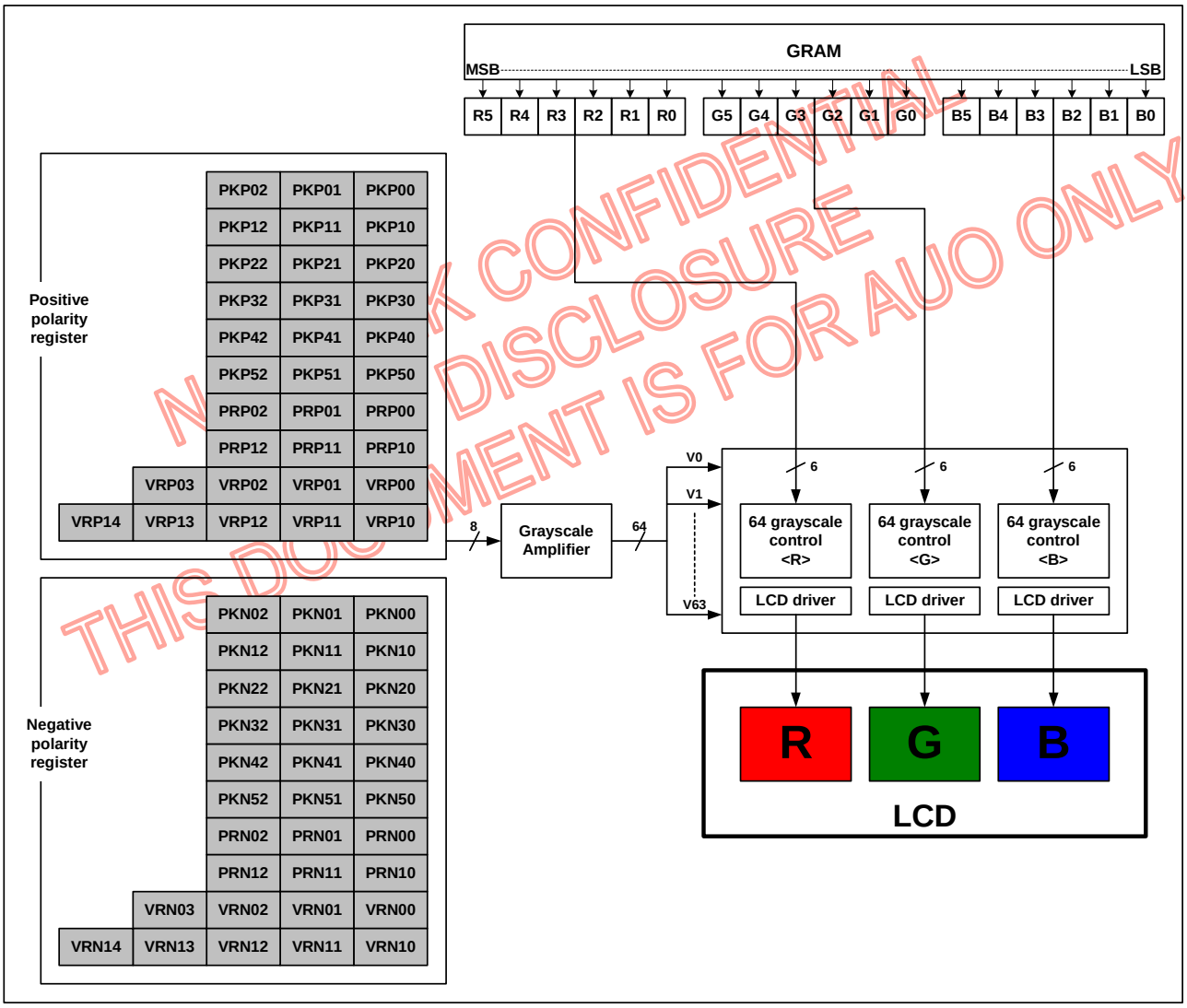
NT3915 gate scan mode is set by SM and GS bit. GS bit determines the scan direction whether the gate driver scans forward or reverse direction. SM bit determines the method of display division (Even/Odd or Upper/Lower division drive). Using this function, various connections between NT3915 and the liquid crystal panels can be accomplished

SM	GS	Scan Mode	
0	0		G1→G2→G3→ G4→…→G173→ G174→G175→G176
0	1		G176→G175→G174→ G173→…→G4→ G1→G2→G3
1	0		G1→G3→G5→ …→G173→G175→ G2→G4→G6 →…→G174→G176
1	1		G176→G174→ G172→…→G4→G2 →G175→G173→ G171→…→G3→G1

Scan mode setting

GAMMA ADJUSTMENT FUNCTION

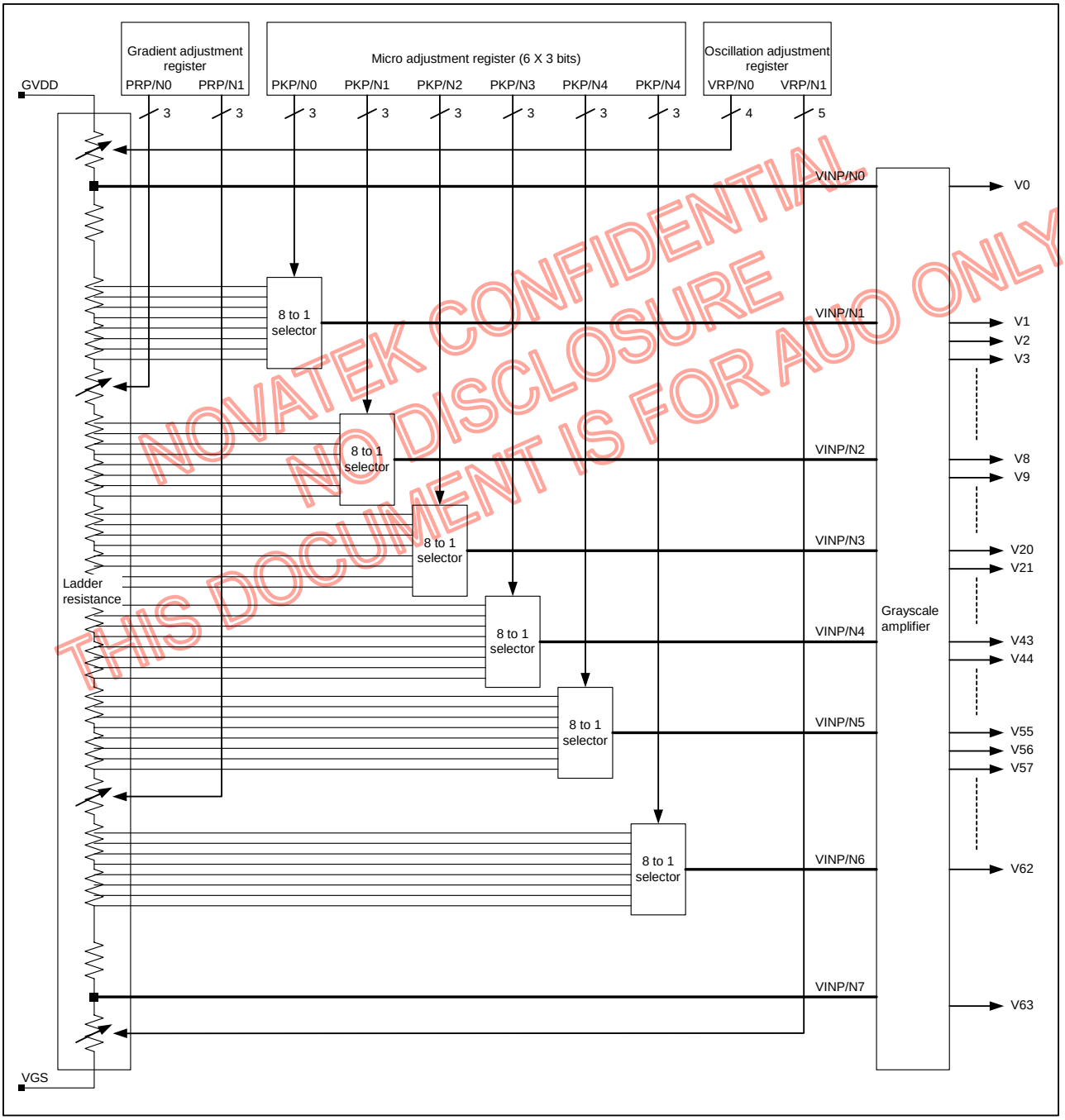
The NT3915 provides the gamma adjustment function to display 262,144 colors simultaneously. The gamma adjustment executed by the gradient adjustment register and the micro-adjustment register that determines 8 grayscale levels. Furthermore, since the gradient adjustment register and the micro-adjustment register have the positive polarities and negative polarities, adjust them to match LCD panel respectively.



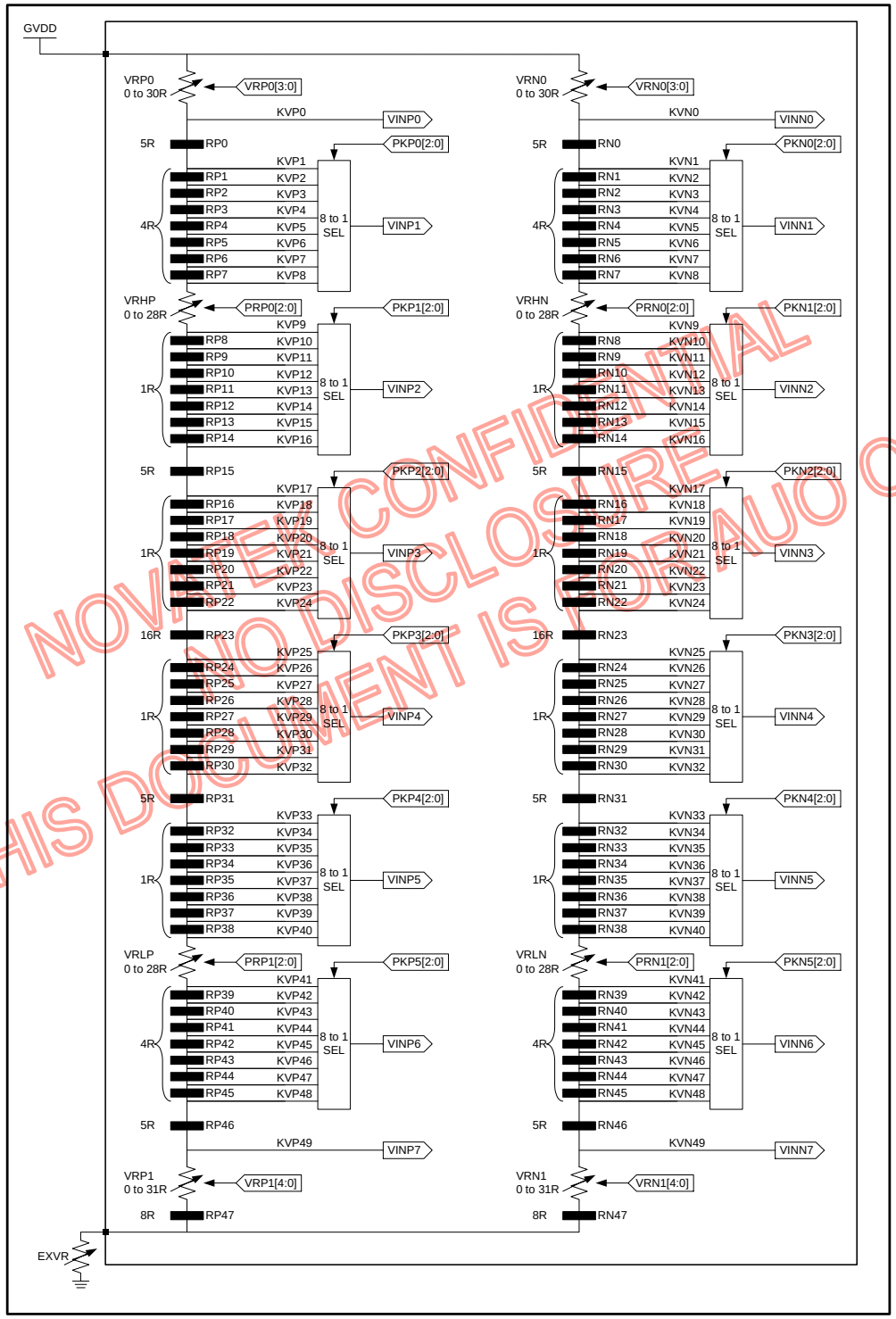
Grayscale control

STRUCTURE OF GRAYSCALE AMPLIFIER

The structure of the grayscale amplifier is shown as below. Determine 8-level (VIN0-VIN7) by the gradient adjuster and the micro adjustment register. Each level is split by the internal ladder resistance and level between V0 to V63 is generated.



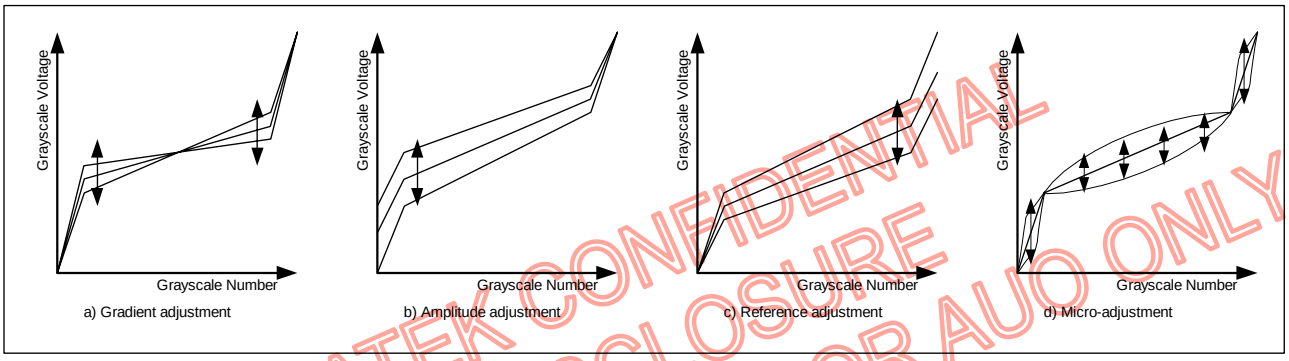
Structure of grayscale amplifier



Structure of Ladder / 8 to 1 selector

GAMMA ADJUSTMENT REGISTER

This block has the register to set up the grayscale voltage adjusting to the gamma specification of the LCD panel. These registers can independently set up to positive/negative polarities and there are 4-type of register groups to adjust gradient and amplitude on number of the grayscale, characteristics of the grayscale voltage. (average <R><G><B> are common.) The following figure indicates the operation of each adjusting register.



The operation of adjusting register

a) Gradient adjustment resistor
The gradient adjustment resistors are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. To accomplish the adjustment, it controls the variable resistor (VRHP (N) / VRLP (N)) of the ladder resistor for the grayscale voltage generator. Also, there is an independent resistor on the positive/negative polarities in order for corresponding to asymmetry drive.

b) Amplitude adjustment resistor
The Amplitude-adjusting resistor is to adjust amplitude of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)1) of the ladder resistor for the grayscale voltage generator located at lower side of the ladder resistor.

c) Reference adjustment resistor
The Reference-adjusting resistor is to adjust reference of the grayscale voltage. To accomplish the adjustment, it controls the variable resistor (VRP(N)0) of the ladder resistor for the grayscale voltage generator located at upper side of the ladder resistor.

d) Micro adjustment resistor
The micro adjustment resistor is to make subtle adjustment of the grayscale voltage level. To accomplish the adjustment, it controls the each reference voltage level by the 8 to 1 selector towards the 8-leveled reference voltage generated from the ladder resistor. Also, there is an independent resistor on the positive/negative polarities as well as other adjusting resistors.

Register	Positive polarity	Negative polarity	Set-up contents
Gradient adjustment	PRP0[2:0]	PRN0[2:0]	Variable resistor VRHP(N)
	PRP1[2:0]	PRN1[2:0]	Variable resistor VRLP(N)
Amplitude adjustment	VRP0[3:0]	VRN0[3:0]	Variable resistor VRP(N)0
	VRP1[4:0]	VRN1[4:0]	Variable resistor VRP(N)1
Micro adjustment	PKP0[2:0]	PKN0[2:0]	The voltage of grayscale number 1 is selected by the 8 to 1 selector
	PKP1[2:0]	PKN1[2:0]	The voltage of grayscale number 8 is selected by the 8 to 1 selector
	PKP2[2:0]	PKN2[2:0]	The voltage of grayscale number 20 is selected by the 8 to 1 selector
	PKP3[2:0]	PKN3[2:0]	The voltage of grayscale number 43 is selected by the 8 to 1 selector
	PKP4[2:0]	PKN4[2:0]	The voltage of grayscale number 55 is selected by the 8 to 1 selector
	PKP5[2:0]	PKN5[2:0]	The voltage of grayscale number 62 is selected by the 8 to 1 selector

Table 16. Gamma correction registers

LADDER RESISTOR / 8 TO 1 SELECTOR

This block outputs the reference voltage of the grayscale voltage. There are two ladder resistors including the variable resistor and the 8 to 1 selector selecting voltage generated by the ladder resistance voltage. The variable and 8 to 1 resistors are controlled by the gamma resistor. Also, there are pins that connect to the external volume resistor. And it allows compensating the dispersion of length between one panel to another.

VARIABLE RESISTOR

There are 2 types of the variable resistors that is for the gradient adjustment (VRHP (N) / VRLP (N)) and for the oscillation adjustment (VRP (N)0/VRP (N)1). The resistance value is set by the gradient adjusting resistor and the oscillation adjustiment resistor as below.

Register value PRP(N)0 [2:0]	Resistance value VRHP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 17. Gradient Adjustment (1)

Register value PRP(N)1 [2:0]	Resistance value VRLP(N)
000	0R
001	4R
010	8R
011	12R
100	16R
101	20R
110	24R
111	28R

Table 18. Gradient Adjustment (2)

Register value VRP(N)0 [3:0]	Resistance value VRP(N)0
0000	0R
0001	2R
0010	4R
:	:
:	:
1101	26R
1110	28R
1111	30R

Table 19. Amplitude Adjustment (1)

Register value VRP(N)1[4:0]	Resistance value VRP(N)1
00000	0R
00001	1R
00010	2R
:	:
:	:
11101	29R
11110	30R
11111	31R

Table 20. Amplitude Adjustment (2)

THE 8 TO 1 SELECTOR

In the 8 to 1 selector, the voltage level must be selected given by the ladder resistance and the micro-adjusting register. And output the voltage the six types of the reference voltage, the VIN1- to VIN6. Following figure explains the relationship between the micro-adjusting register and the selecting voltage.

Register value PKP(N) [2:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
000	KVP(N)1	KVP(N)9	KVP(N)17	KVP(N)25	KVP(N)33	KVP(N)41
001	KVP(N)2	KVP(N)10	KVP(N)18	KVP(N)26	KVP(N)34	KVP(N)42
010	KVP(N)3	KVP(N)11	KVP(N)19	KVP(N)27	KVP(N)35	KVP(N)43
011	KVP(N)4	KVP(N)12	KVP(N)20	KVP(N)28	KVP(N)36	KVP(N)44
100	KVP(N)5	KVP(N)13	KVP(N)21	KVP(N)29	KVP(N)37	KVP(N)45
101	KVP(N)6	KVP(N)14	KVP(N)22	KVP(N)30	KVP(N)38	KVP(N)46
110	KVP(N)7	KVP(N)15	KVP(N)23	KVP(N)31	KVP(N)39	KVP(N)47
111	KVP(N)8	KVP(N)16	KVP(N)24	KVP(N)32	KVP(N)40	KVP(N)48

Table 21. Relationship between Micro-adjustment Register and Selected Voltage

Pins	Formula	Micro-adjusting register value	Reference voltage
KVP0	VINP0	-	VINP0
KVP1	VINP0-ΔV*5R/SUMRP	PKP02-00 = “000”	VINP1
KVP2	VINP0-ΔV*9R/SUMRP	PKP02-00 = “001”	
KVP3	VINP0-ΔV*13R/SUMRP	PKP02-00 = “010”	
KVP4	VINP0-ΔV*17R/SUMRP	PKP02-00 = “011”	
KVP5	VINP0-ΔV*21R/SUMRP	PKP02-00 = “100”	
KVP6	VINP0-ΔV*25R/SUMRP	PKP02-00 = “101”	
KVP7	VINP0-ΔV*29R/SUMRP	PKP02-00 = “110”	
KVP8	VINP0-ΔV*33R/SUMRP	PKP02-00 = “111”	
KVP9	VINP0-ΔV*(33R+VRHP)/SUMRP	PKP12-10 = “000”	VINP2
KVP10	VINP0-ΔV*(34R+VRHP)/SUMRP	PKP12-10 = “001”	
KVP11	VINP0-ΔV*(35R+VRHP)/SUMRP	PKP12-10 = “010”	
KVP12	VINP0-ΔV*(36R+VRHP)/SUMRP	PKP12-10 = “011”	
KVP13	VINP0-ΔV*(37R+VRHP)/SUMRP	PKP12-10 = “100”	
KVP14	VINP0-ΔV*(38R+VRHP)/SUMRP	PKP12-10 = “101”	
KVP15	VINP0-ΔV*(39R+VRHP)/SUMRP	PKP12-10 = “110”	
KVP16	VINP0-ΔV*(40R+VRHP)/SUMRP	PKP12-10 = “111”	
KVP17	VINP0-ΔV*(45R+VRHP)/SUMRP	PKP22-20 = “000”	VINP3
KVP18	VINP0-ΔV*(46R+VRHP)/SUMRP	PKP22-20 = “001”	
KVP19	VINP0-ΔV*(47R+VRHP)/SUMRP	PKP22-20 = “010”	
KVP20	VINP0-ΔV*(48R+VRHP)/SUMRP	PKP22-20 = “011”	
KVP21	VINP0-ΔV*(49R+VRHP)/SUMRP	PKP22-20 = “100”	
KVP22	VINP0-ΔV*(50R+VRHP)/SUMRP	PKP22-20 = “101”	
KVP23	VINP0-ΔV*(51R+VRHP)/SUMRP	PKP22-20 = “110”	
KVP24	VINP0-ΔV*(52R+VRHP)/SUMRP	PKP22-20 = “111”	
KVP25	VINP0-ΔV*(68R+VRHP)/SUMRP	PKP32-30 = “000”	VINP4
KVP26	VINP0-ΔV*(69R+VRHP)/SUMRP	PKP32-30 = “001”	
KVP27	VINP0-ΔV*(70R+VRHP)/SUMRP	PKP32-30 = “010”	
KVP28	VINP0-ΔV*(71R+VRHP)/SUMRP	PKP32-30 = “011”	
KVP29	VINP0-ΔV*(72R+VRHP)/SUMRP	PKP32-30 = “100”	
KVP30	VINP0-ΔV*(73R+VRHP)/SUMRP	PKP32-30 = “101”	
KVP31	VINP0-ΔV*(74R+VRHP)/SUMRP	PKP32-30 = “110”	
KVP32	VINP0-ΔV*(75R+VRHP)/SUMRP	PKP32-30 = “111”	
KVP33	VINP0-ΔV*(80R+VRHP)/SUMRP	PKP42-40 = “000”	VINP5
KVP34	VINP0-ΔV*(81R+VRHP)/SUMRP	PKP42-40 = “001”	
KVP35	VINP0-ΔV*(82R+VRHP)/SUMRP	PKP42-40 = “010”	
KVP36	VINP0-ΔV*(83R+VRHP)/SUMRP	PKP42-40 = “011”	
KVP37	VINP0-ΔV*(84R+VRHP)/SUMRP	PKP42-40 = “100”	
KVP38	VINP0-ΔV*(85R+VRHP)/SUMRP	PKP42-40 = “101”	
KVP39	VINP0-ΔV*(86R+VRHP)/SUMRP	PKP42-40 = “110”	
KVP40	VINP0-ΔV*(87R+VRHP)/SUMRP	PKP42-40 = “111”	
KVP41	VINP0-ΔV*(87R+VRHP+VRLP)/SUMRP	PKP52-50 = “000”	VINP6
KVP42	VINP0-ΔV*(91R+VRHP+VRLP)/SUMRP	PKP52-50 = “001”	
KVP43	VINP0-ΔV*(95R+VRHP+VRLP)/SUMRP	PKP52-50 = “010”	
KVP44	VINP0-ΔV*(99R+VRHP+VRLP)/SUMRP	PKP52-50 = “011”	
KVP45	VINP0-ΔV*(103R+VRHP+VRLP)/SUMRP	PKP52-50 = “100”	
KVP46	VINP0-ΔV*(107R+VRHP+VRLP)/SUMRP	PKP52-50 = “101”	
KVP47	VINP0-ΔV*(111R+VRHP+VRLP)/SUMRP	PKP52-50 = “110”	
KVP48	VINP0-ΔV*(115R+VRHP+VRLP)/SUMRP	PKP52-50 = “111”	
KVP49	VINP0-ΔV*(120R+VRHP+VRLP)/SUMRP	-	VINP7

Table 22. Gamma Adjusting Voltage Formula (Positive Polarity) 1

SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0+VRP1
SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0+VRN1
VINP0=GVDD-ΔV*VRP0/SUMRP
ΔV: Potential difference between GVDD and VGS = GVDD*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	V43+(V20-V43)*(11/23)
V1	VINP1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINP2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINP4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINP3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINP5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINP6
V31	V43+(V20-V43)*(12/23)	V63	VINP7

Table 23. Gamma Voltage Formula (Positive Polarity) 2

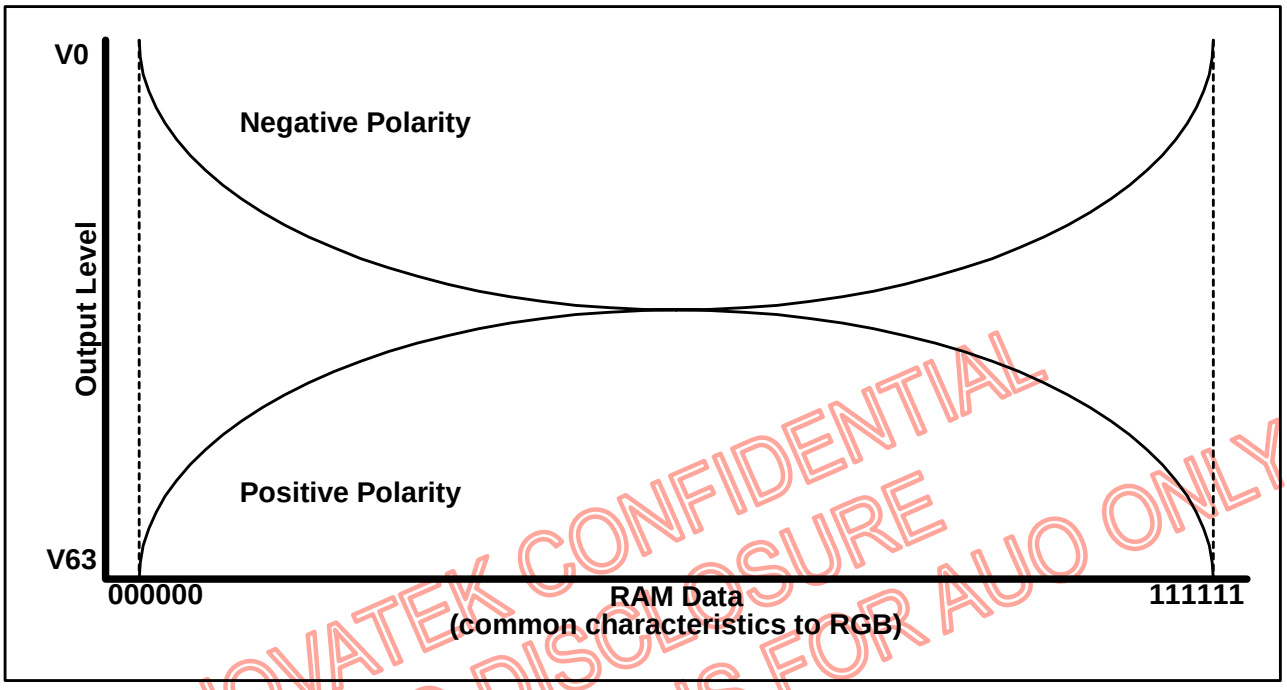
Pins	Formula	Micro-adjusting register value	Reference voltage
KVN0	VINN0	-	VINN0
KVN1	VINN0-ΔV*5R/SUMRN	PKN02-00 = “000”	VINN1
KVN2	VINN0-ΔV*9R/SUMRN	PKN02-00 = “001”	
KVN3	VINN0-ΔV*13R/SUMRN	PKN02-00 = “010”	
KVN4	VINN0-ΔV*17R/SUMRN	PKN02-00 = “011”	
KVN5	VINN0-ΔV*21R/SUMRN	PKN02-00 = “100”	
KVN6	VINN0-ΔV*25R/SUMRN	PKN02-00 = “101”	
KVN7	VINN0-ΔV*29R/SUMRN	PKN02-00 = “110”	
KVN8	VINN0-ΔV*33R/SUMRN	PKN02-00 = “111”	
KVN9	VINN0-ΔV*(33R+VRHN)/SUMRN	PKN12-10 = “000”	VINN2
KVN10	VINN0-ΔV*(34R+VRHN)/SUMRN	PKN12-10 = “001”	
KVN11	VINN0-ΔV*(35R+VRHN)/SUMRN	PKN12-10 = “010”	
KVN12	VINN0-ΔV*(36R+VRHN)/SUMRN	PKN12-10 = “011”	
KVN13	VINN0-ΔV*(37R+VRHN)/SUMRN	PKN12-10 = “100”	
KVN14	VINN0-ΔV*(38R+VRHN)/SUMRN	PKN12-10 = “101”	
KVN15	VINN0-ΔV*(39R+VRHN)/SUMRN	PKN12-10 = “110”	
KVN16	VINN0-ΔV*(40R+VRHN)/SUMRN	PKN12-10 = “111”	
KVN17	VINN0-ΔV*(45R+VRHN)/SUMRN	PKN22-20 = “000”	VINN3
KVN18	VINN0-ΔV*(46R+VRHN)/SUMRN	PKN22-20 = “001”	
KVN19	VINN0-ΔV*(47R+VRHN)/SUMRN	PKN22-20 = “010”	
KVN20	VINN0-ΔV*(48R+VRHN)/SUMRN	PKN22-20 = “011”	
KVN21	VINN0-ΔV*(49R+VRHN)/SUMRN	PKN22-20 = “100”	
KVN22	VINN0-ΔV*(50R+VRHN)/SUMRN	PKN22-20 = “101”	
KVN23	VINN0-ΔV*(51R+VRHN)/SUMRN	PKN22-20 = “110”	
KVN24	VINN0-ΔV*(52R+VRHN)/SUMRN	PKN22-20 = “111”	
KVN25	VINN0-ΔV*(68R+VRHN)/SUMRN	PKN32-30 = “000”	VINN4
KVN26	VINN0-ΔV*(69R+VRHN)/SUMRN	PKN32-30 = “001”	
KVN27	VINN0-ΔV*(70R+VRHN)/SUMRN	PKN32-30 = “010”	
KVN28	VINN0-ΔV*(71R+VRHN)/SUMRN	PKN32-30 = “011”	
KVN29	VINN0-ΔV*(72R+VRHN)/SUMRN	PKN32-30 = “100”	
KVN30	VINN0-ΔV*(73R+VRHN)/SUMRN	PKN32-30 = “101”	
KVN31	VINN0-ΔV*(74R+VRHN)/SUMRN	PKN32-30 = “110”	
KVN32	VINN0-ΔV*(75R+VRHN)/SUMRN	PKN32-30 = “111”	
KVN33	VINN0-ΔV*(80R+VRHN)/SUMRN	PKN42-40 = “000”	VINN5
KVN34	VINN0-ΔV*(81R+VRHN)/SUMRN	PKN42-40 = “001”	
KVN35	VINN0-ΔV*(82R+VRHN)/SUMRN	PKN42-40 = “010”	
KVN36	VINN0-ΔV*(83R+VRHN)/SUMRN	PKN42-40 = “011”	
KVN37	VINN0-ΔV*(84R+VRHN)/SUMRN	PKN42-40 = “100”	
KVN38	VINN0-ΔV*(85R+VRHN)/SUMRN	PKN42-40 = “101”	
KVN39	VINN0-ΔV*(86R+VRHN)/SUMRN	PKN42-40 = “110”	
KVN40	VINN0-ΔV*(87R+VRHN)/SUMRN	PKN42-40 = “111”	
KVN41	VINN0-ΔV*(87R+VRHN+VRLN)/SUMRN	PKN52-50 = “000”	VINN6
KVN42	VINN0-ΔV*(91R+VRHN+VRLN)/SUMRN	PKN52-50 = “001”	
KVN43	VINN0-ΔV*(95R+VRHN+VRLN)/SUMRN	PKN52-50 = “010”	
KVN44	VINN0-ΔV*(99R+VRHN+VRLN)/SUMRN	PKN52-50 = “011”	
KVN45	VINN0-ΔV*(103R+VRHN+VRLN)/SUMRN	PKN52-50 = “100”	
KVN46	VINN0-ΔV*(107R+VRHN+VRLN)/SUMRN	PKN52-50 = “101”	
KVN47	VINN0-ΔV*(111R+VRHN+VRLN)/SUMRN	PKN52-50 = “110”	
KVN48	VINN0-ΔV*(115R+VRHN+VRLN)/SUMRN	PKN52-50 = “111”	
KVN49	VINN0-ΔV*(120R+VRHN+VRLN)/SUMRN	-	VINN7

Table 24. Gamma Adjusting Voltage Formula (Negative Polarity) 1

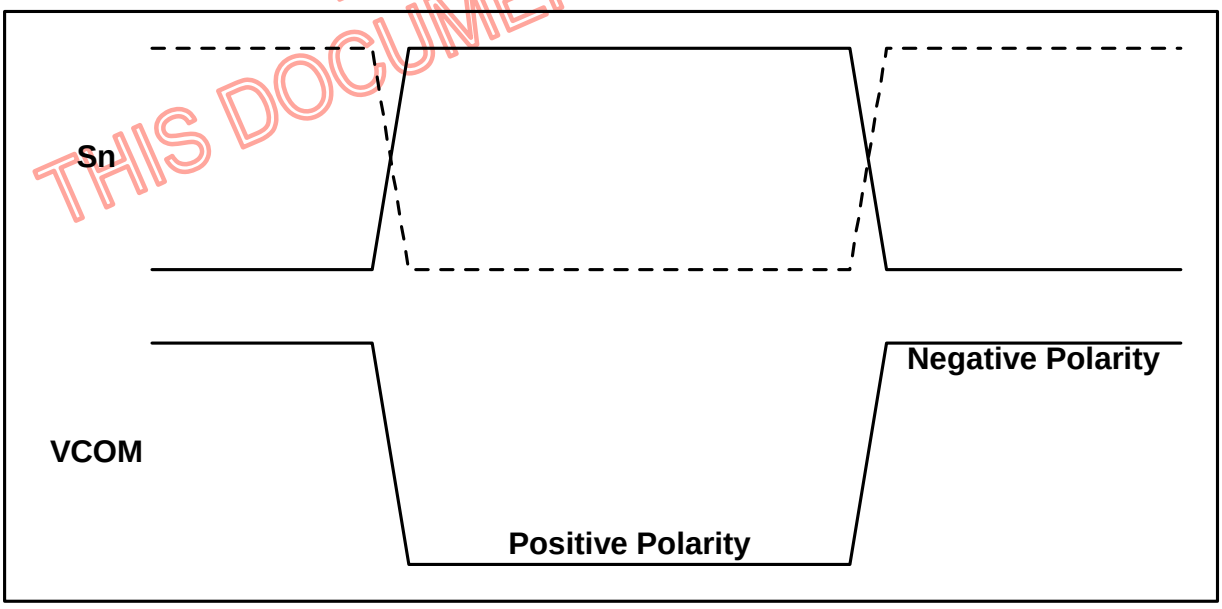
SUMRP: Total of the positive polarity ladder resistance = 128R + VRHP + VRLP + VRP0+VRP1
SUMRN: Total of the negative polarity ladder resistance = 128R + VRHN + VRLN + VRN0+VRN1
VINN0=GVDD-ΔV*VRN0/SUMRN
ΔV: Potential difference between GVDD and VGS = GVDD*SUMRP*SUMRN / [SUMRP*SUMRN+EXVR*(SUMRP+SUMRN)]

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	V43+(V20-V43)*(11/23)
V1	VINN1	V33	V43+(V20-V43)*(10/23)
V2	V3+(V1-V3)*(8/24)	V34	V43+(V20-V43)*(9/23)
V3	V8+(V1-V8)*(450/800)	V35	V43+(V20-V43)*(8/23)
V4	V8+(V3-V8)*(16/24)	V36	V43+(V20-V43)*(7/23)
V5	V8+(V3-V8)*(12/24)	V37	V43+(V20-V43)*(6/23)
V6	V8+(V3-V8)*(8/24)	V38	V43+(V20-V43)*(5/23)
V7	V8+(V3-V8)*(4/24)	V39	V43+(V20-V43)*(4/23)
V8	VINN2	V40	V43+(V20-V43)*(3/23)
V9	V20+(V8-V20)*(22/24)	V41	V43+(V20-V43)*(2/23)
V10	V20+(V8-V20)*(20/24)	V42	V43+(V20-V43)*(1/23)
V11	V20+(V8-V20)*(18/24)	V43	VINN4
V12	V20+(V8-V20)*(16/24)	V44	V55+(V43-V55)*(22/24)
V13	V20+(V8-V20)*(14/24)	V45	V55+(V43-V55)*(20/24)
V14	V20+(V8-V20)*(12/24)	V46	V55+(V43-V55)*(18/24)
V15	V20+(V8-V20)*(10/24)	V47	V55+(V43-V55)*(16/24)
V16	V20+(V8-V20)*(8/24)	V48	V55+(V43-V55)*(14/24)
V17	V20+(V8-V20)*(6/24)	V49	V55+(V43-V55)*(12/24)
V18	V20+(V8-V20)*(4/24)	V50	V55+(V43-V55)*(10/24)
V19	V20+(V8-V20)*(2/24)	V51	V55+(V43-V55)*(8/24)
V20	VINN3	V52	V55+(V43-V55)*(6/24)
V21	V43+(V20-V43)*(22/23)	V53	V55+(V43-V55)*(4/24)
V22	V43+(V20-V43)*(21/23)	V54	V55+(V43-V55)*(2/24)
V23	V43+(V20-V43)*(20/23)	V55	VINN5
V24	V43+(V20-V43)*(19/23)	V56	V60+(V55-V60)*(20/24)
V25	V43+(V20-V43)*(18/23)	V57	V60+(V55-V60)*(16/24)
V26	V43+(V20-V43)*(17/23)	V58	V60+(V55-V60)*(12/24)
V27	V43+(V20-V43)*(16/23)	V59	V60+(V55-V60)*(8/24)
V28	V43+(V20-V43)*(15/23)	V60	V62+(V55-V62)*(350/800)
V29	V43+(V20-V43)*(14/23)	V61	V62+(V60-V62)*(16/24)
V30	V43+(V20-V43)*(13/23)	V62	VINN6
V31	V43+(V20-V43)*(12/23)	V63	VINN7

Table 25. Gamma Voltage Formula (Negative Polarity) 2



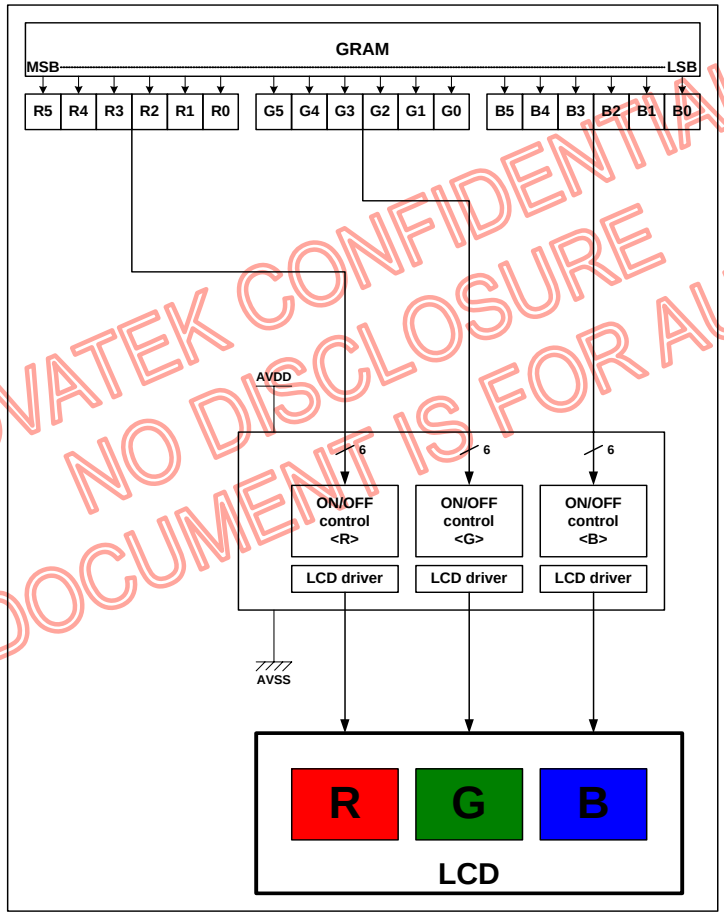
Relationship between RAM data and output voltage



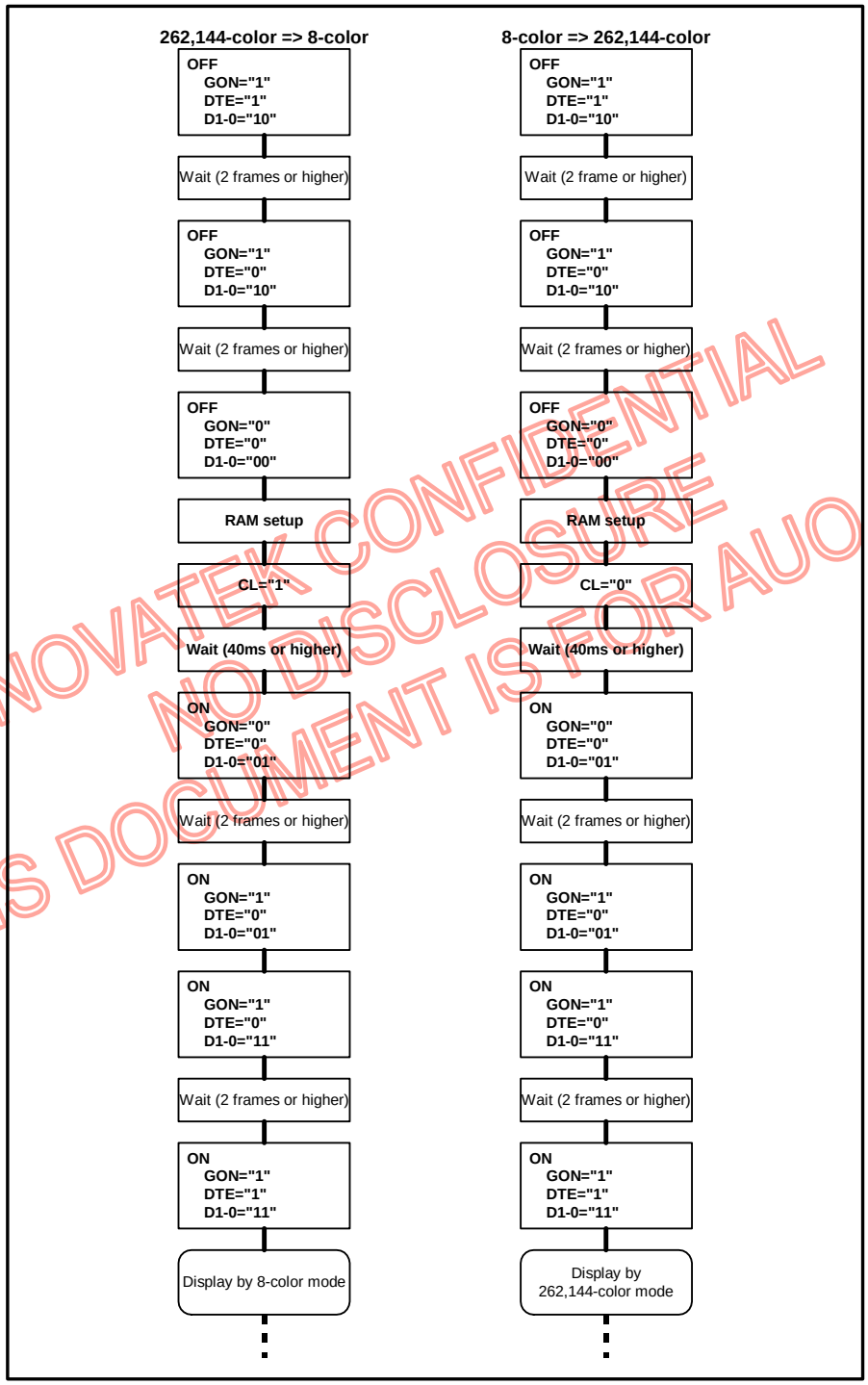
Relationship between source output and Vcom

THE 8-COLOR DISPLAY MODE

The NT3915 incorporates 8-color display mode. The grayscale levels to be used is AVDD and AVSS and all the other levels (V0~V63) are halt. So that it attempts to lower power consumption.
During the 8-color mode, the Gamma gradient, amplitude, reference, and micro adjustment register are invalid. Since V0-V63 is stopped, the RGB data in the GRAM should be set to 000000 or 111111 before set the mode. The level power supply (V0-V63) is in OFF condition during the 8-color mode in order to select AVDD/AVSS.

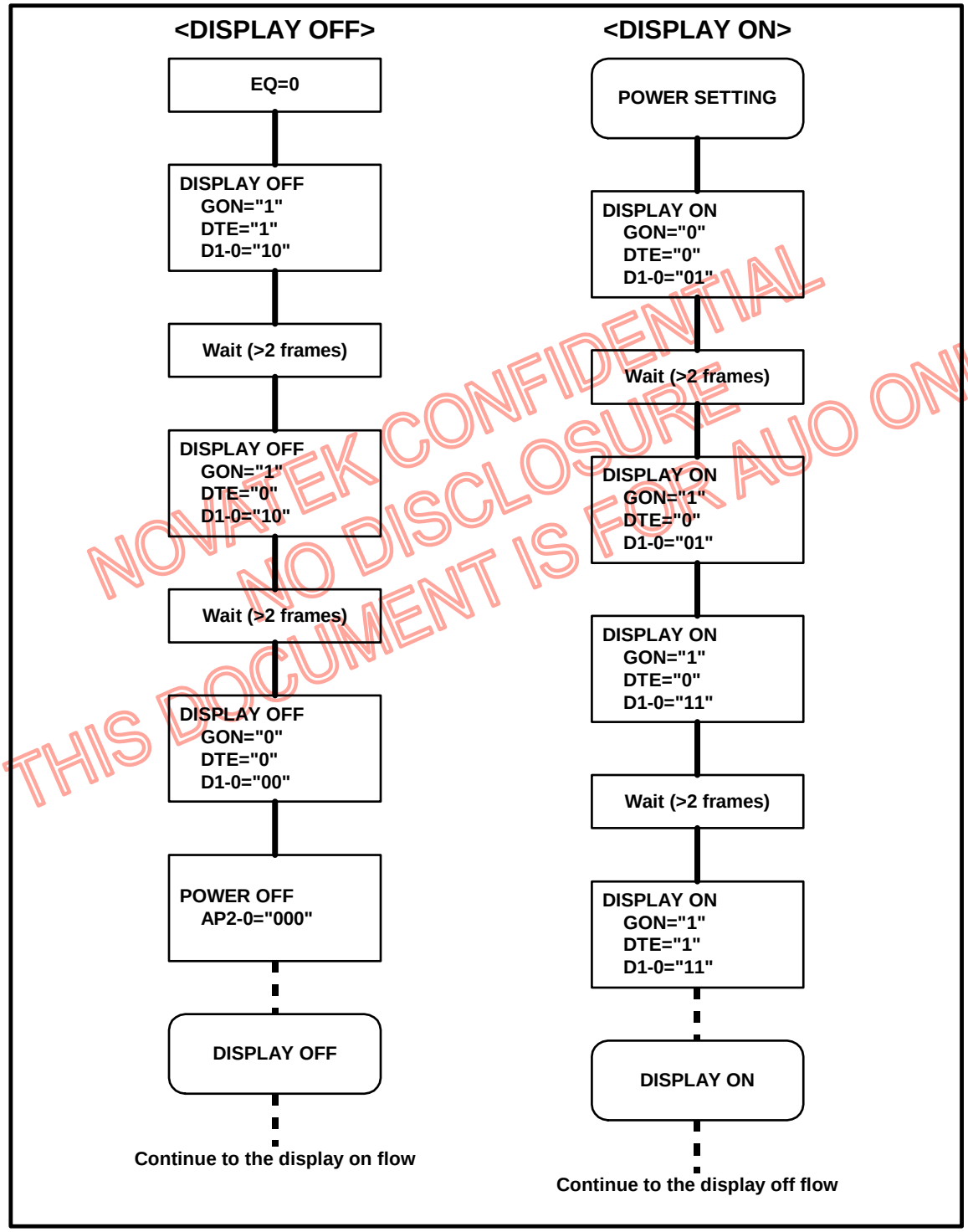


8-color display control

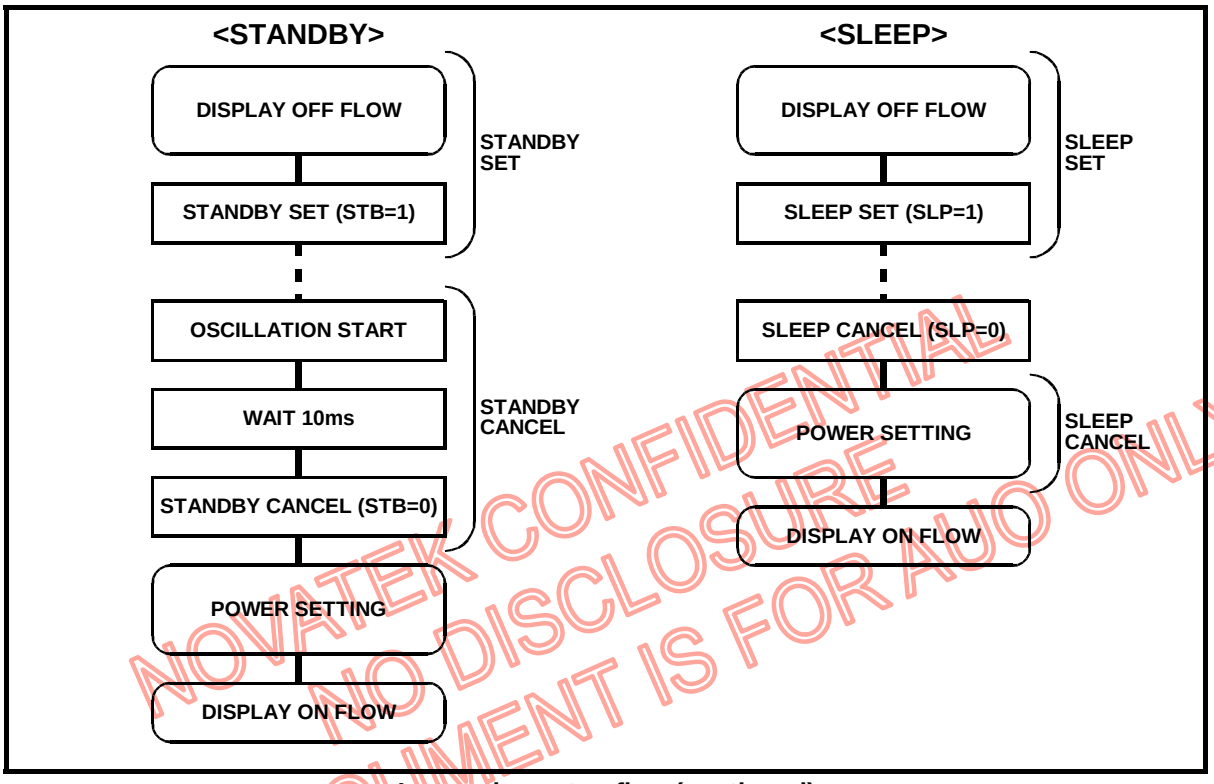


Set up procedure for the 8-color mode

Instruction set up flow



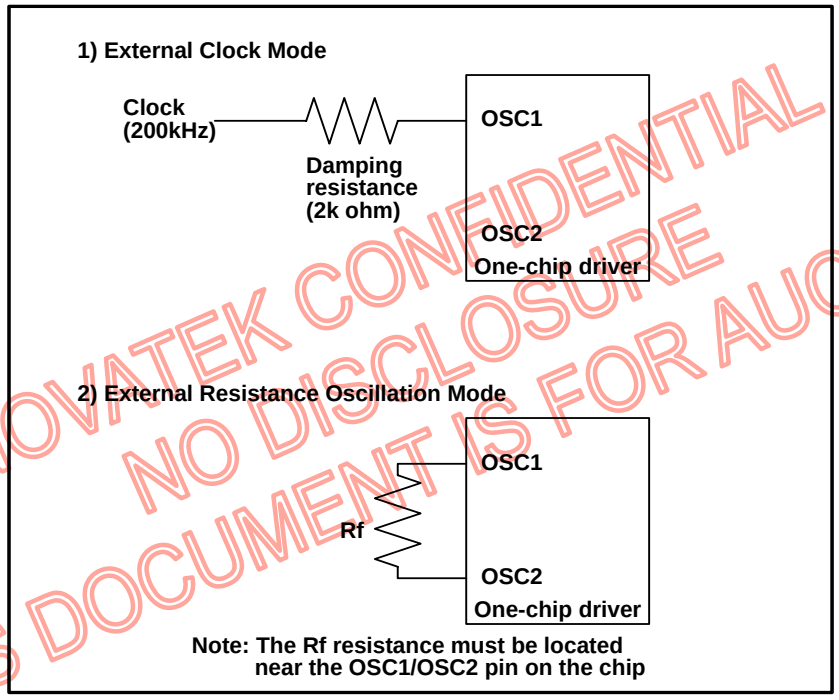
Instruction set up flow



Instruction setup flow (continued)

OSCILLATION CIRCUIT

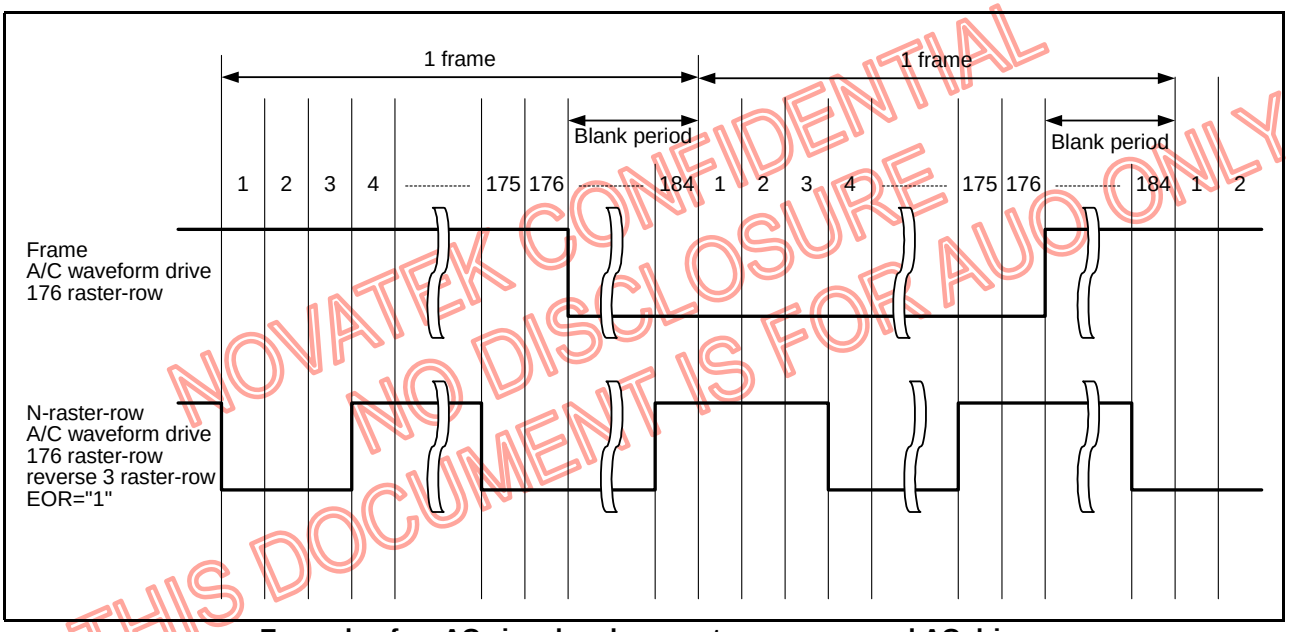
The NT3915 can oscillate between the OSC1 and OSC2 pins using an internal R-C oscillator with an external oscillation resistor. Note that in R-C oscillation, the oscillation frequency is changed according to the external resistance value, wiring length, or operating power-supply voltage. If Rf is increased or power supply voltage is decrease, the oscillation frequency decreases. For the relationship between Rf resistor value and oscillation frequency, see the Electric Characteristics Notes section.



Oscillation Circuit

N-RASTER-ROW REVERSED AC DRIVE

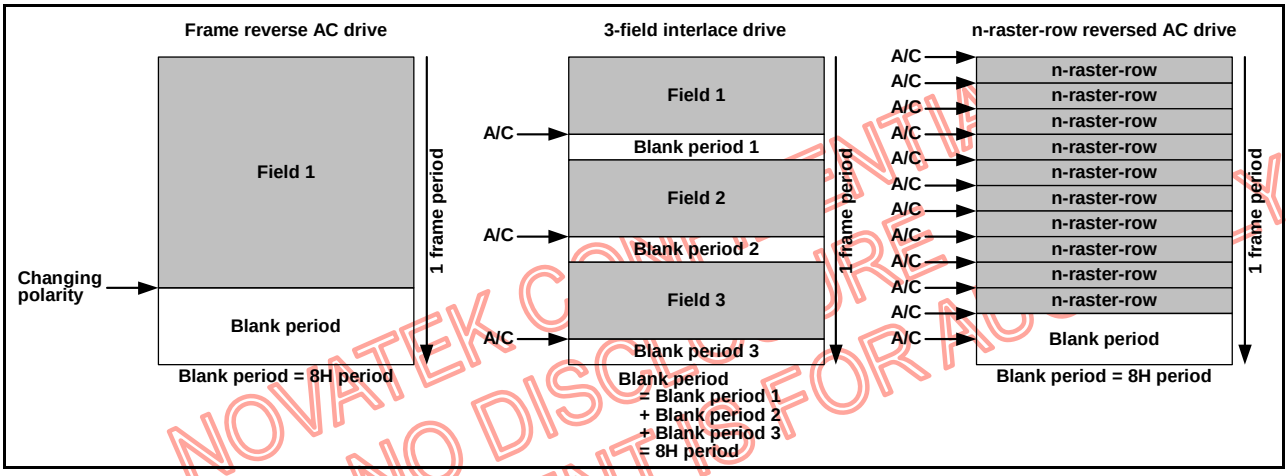
The NT3915 supports not only the LCD reversed AC drive in a one-frame unit but also the n-raster-row reversed AC drive which alternates in an n-raster-row unit from one to 64 raster-rows. When a problem affecting display quality occurs, the n-raster-row reversed AC drive can improve the quality.
Determine the number of the raster-rows n (NW bit set value +1) for alternating after confirmation of the display quality with the actual LCD panel. However, if the number of AC raster-row is reduced, the LCD alternating frequency becomes high. Because of this, the charge or discharge current is increased in the LCD cells.



Example of an AC signal under n-raster-row reversed AC drive

A/C TIMING

Following diagram indicates the A/C timing on the each A/C drive method. After every 1 drawing, the A/C timing is occurred on the reversed frame AC drive. After the A/C timing, the blank (all gate output: Vgoff level) period described below is inserted. When it is on the interlace drive, blank period is inserted every A/C timing. When the reversed n-raster-row is driving, a blank period is inserted after all screens are drawn. The amount of blanking period becomes 8H in a frame. When the reversed is driving, a blank period of the 8H period in inserted after all screens are drawn.



A/C timing

INTERLACE DRIVE

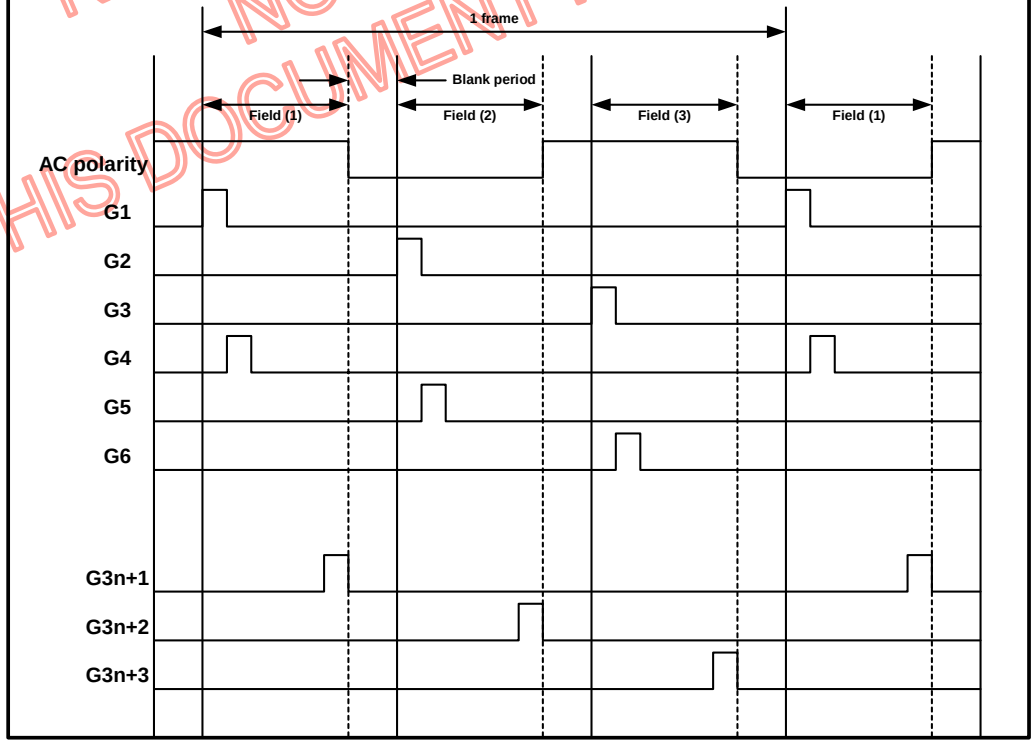
NT3915 supports the interlace drive to protect from the flicker. It splits one frame into n fields and drives. Determine the n fields (FLD bit stetting value) after confirming on the actual LCD display. Following table indicates n fields: the gate selecting position when it is 1 or 3. and the diagram below indicates the output waveform when the field interlace drive is active.

GS="0"

FLD1-0 setting value	01	11		
Gate \ Field	—	(1)	(2)	(3)
G1	O	O		
G2	O		O	
G3	O			O
G4	O	O		
G5	O		O	
G6	O			O
G7	O	O		
G8	O		O	
G9	O			O
⋮	⋮	⋮	⋮	⋮
G173	O		O	
G174	O			O
G175	O	O		
G176	O		O	

GS="1"

FLD1-0 setting value	01	11		
Gate \ Field	—	(1)	(2)	(3)
G176	O	O		
G175	O		O	
G174	O			O
G173	O	O		
G172	O		O	
G171	O			O
G170	O	O		
G169	O		O	
G168	O			O
⋮	⋮	⋮	⋮	⋮
G4	O		O	
G3	O			O
G2	O	O		
G1	O		O	



Interlace drive and output waveform

FRAME FREQUENCY ADJUSTING FUNCTION

The NT3915 has an on-chip frame-frequency adjustment function. The frame frequency can be adjusted by the instruction setting (DIV, RTN) during the LCD driver as the oscillation frequency is always same.
If the oscillation frequency is set to high, animation or a static image can be displayed in suitable ways by changing the frame frequency. When a static image is displayed, the frame frequency can be set low and the low-power consumption mode can be entered. When high-speed screen switching for an animated display, etc. is required, the frame frequency can be set high.

RELATIONSHIP BETWEEN LCD DRIVE DUTY AND FRAME FREQUENCY

The relationships between the LCD drive duty and the frame frequency is calculated by the following expression. The frame frequency can be adjusted in the 1H period adjusting bit (RTN) and in the operation clock division bit (DIV) by the instruction.

$$Frame\quad Frequency = \frac{f_{osc}}{\text{Clock cycles per raster - row} \times \text{Division ratio} \times (\text{Line} + 8)}[Hz]$$

f_{osc}: R-C oscillation frequency
Line: Number of raster-rows (NL bit)
Clock cycles per raster-row: RTN bit
Division ratio: DIV bit

Example calculation

Driver raster-row: 176
1H period: 16 clock (RTN3 to 0 = 0000)
Operation clock division ratio: 1division
B: Blank period (BP + FP): 8
fosc = 60Hz x (0+16) clock x 1 division x (176+B) lines = 177 [kHz]

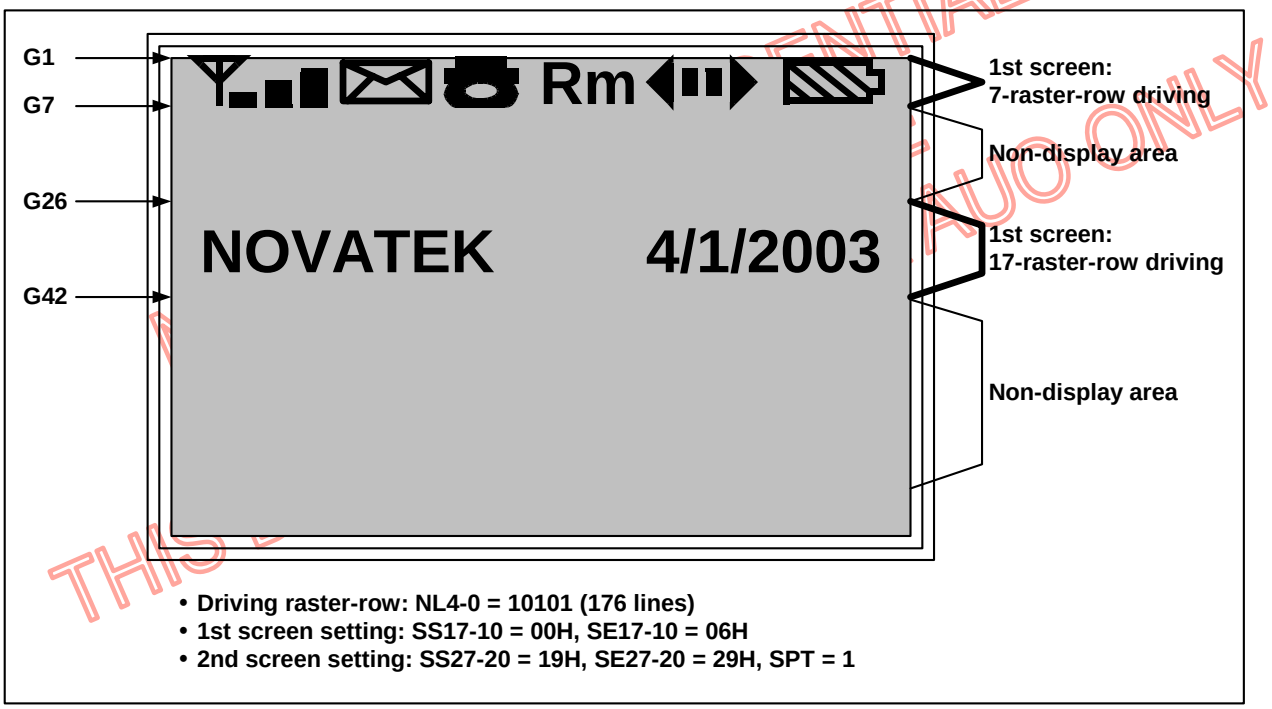
In this case, the RC oscillation frequency becomes 177 kHz. The external resistance value of the RC oscillator must be adjusted to be 177 kHz.

Note: When FLD1-0=”11”(interlace drive), B = BP + FP + BLP1 + BLP2

SCREEN-DIVISION DRIVING FUNCTION

The NT3915 can select and drive two screens at any position with the screen-driving position registers (R14 and R15). Any two screens required for display are selectively driven and reducing LCD-driving voltage and power consumption.

For the 1st division screen, start line (SS17 to 10) and end line (SE17 to 10) are specified by the 1st screen-driving position register (R14). For the 2nd division screen, start line (SS27 to 20) and end line (SE27 to 20) are specified by the 2nd screen-driving position register (R15). The 2nd screen control is effective when the SPT bit is 1. The total count of selection-driving lines for the 1st and 2nd screens must correspond to the LCD-driving duty set value.



Driving on 2 screen

RESTRICTION ON THE 1ST/2ND SCREEN DRIVING POSITION REGISTER SETTINGS

The following restrictions must be satisfied when setting the start line (SS17 to 10) and end line (SE17 to 10) of the 1st screen driving position register (R42H) and the start line (SS27 to 20) and end line (SE27 to 20) of the 2nd screen driving position register (R43H) for the NT3915. Note that incorrect display may occur if the restrictions are not satisfied.

1st Screen Driving (SPT=0)

Register setting	Display operation
(SE17 to 10) – (SS17 to 10) = NL	Full screen display Normally displays (SS17 to 10) to (SE17 to 10)
(SE17 to 10) – (SS17 to 10) < NL	Partial display Normally displays (SS17 to 10) to (SE17 to 10) White display for all other times (RAM data is not related at all)
(SE17 to 10) – (SS17 to 10) > NL	Setting disabled

NOTE 1: SS17 to 10 ≤ SE17 to 10 ≤ AFh
NOTE 2: Setting SE27 to 20 and SS27 to 20 are invalid

2nd Screen Driving (SPT=1)

Register setting	Display operation
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) = NL	Full screen display Normally displays (SS27 to 10) to (SE17 to 10)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) < NL	Partial display Normally displays (SS27 to 10) to (SE17 to 10) White display for all other times (RAM data is not related at all)
((SE17 to 10) – (SS17 to 10)) + ((SE27 to 20) – (SS27-20)) > NL	Setting disabled

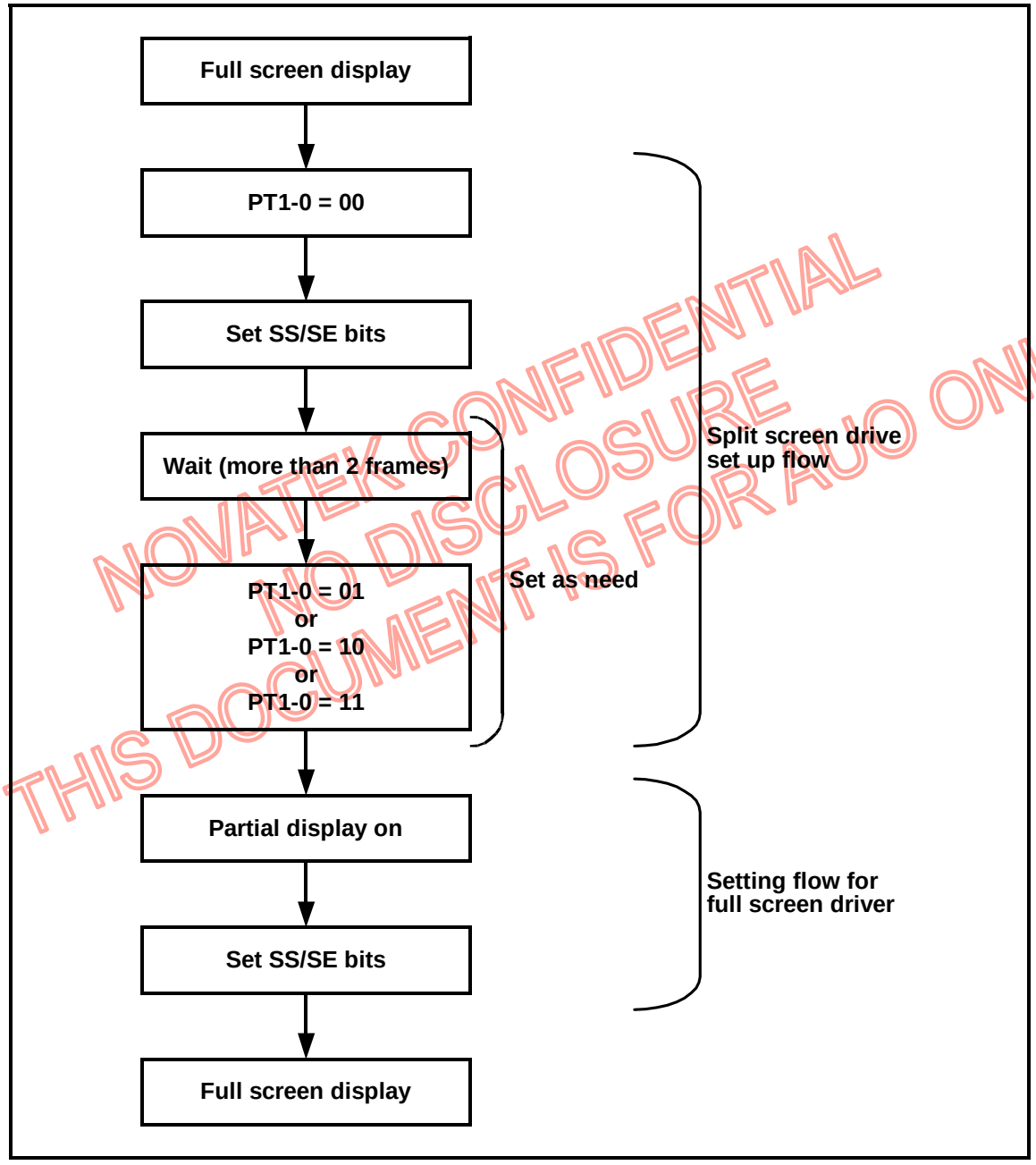
Table 26. Restrictions on the 1st/2nd Screen Driving Position Register Setting

NOTE 1: SS17 to 10 ≤ SE17 to 10 < SS27 to 20 ≤ SE27 to 20 ≤ AFh
NOTE 2: (SE27 to 20) – (SS17 to 10) ≤ NL

The driver output can't be set for non-display area during the partial display. Determine based on specification of the panels.

PT1	PT0	Source output in non-display area		Gate output in Non-display area
		Positive polarity	Negative polarity	
0	0	V63	V0	Normal drive
0	1	V63	V0	Vgoff
1	0	VSS	VSS	Vgoff
1	1	Hi-Z	Hi-Z	Vgoff

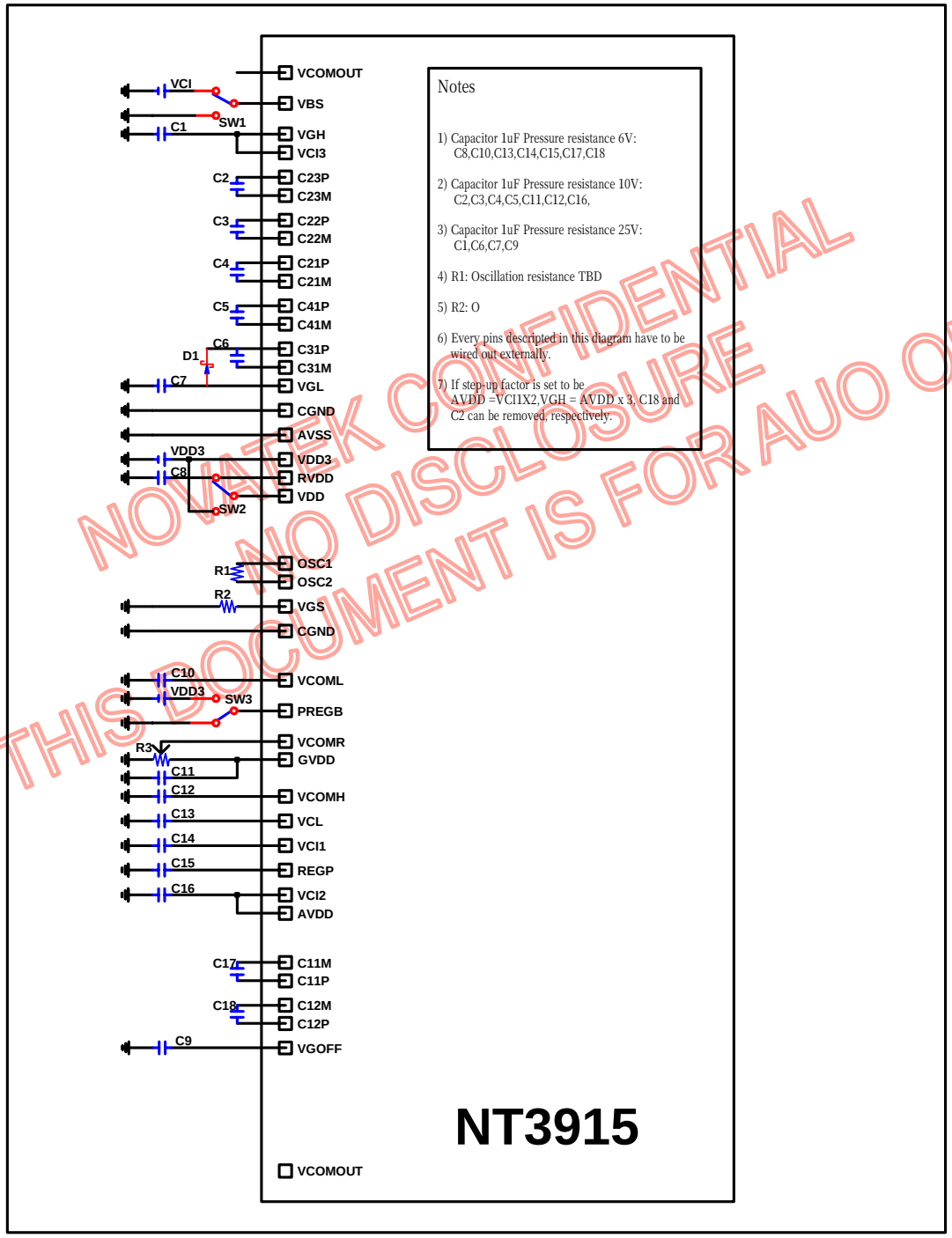
Refer to the following flow to set up the partial display.



Partial display set up flow

APPLICATION CIRCUIT

The following figure indicates a schematic diagram of application circuit for NT3915.



Application Circuit

ABSOLUTE MAXIMUM RATING*

Power supply voltage, VDD3	-0.5V to 5V
Analog supply voltage for charge-pump circuit, VCI	-0.5V to 5V
LCD Supply voltage range, |VGH- VGL|	30V
Digital input voltage range	-0.5V to VDD+0.5V
Storage temperature	-55 °C to 110 °C
Operating temperature	-30 °C to 85 °C

***Comments**

Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability. Operating temperature is the range of device-operating temperature. They do not guarantee chip performance.

DC Electrical Characteristics

(For the digital circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Supply Voltage	VDD	2.0	-	2.5	V	VSS=0, PREGB="H"
	VDD3	2.5	-	3.3	V	VSS=0, PREGB="L"
Low Level Input Voltage	Vil	0	-	0.3xVDD3	V	IM3-0, CSB, E, R/W, RS, DB17-0, PREGB, RESETB1, 2, 3
High Level Input Voltage	Vih	0.7x VDD3	-	VDD3	V	
High Level Output Voltage	Voh	VDD3-0.4	-	-	V	DB17-0, CL1, M, FLM, EQ, DISPTMG, IOH= 400uA
Low Level Output Voltage	Vol	0	-	0.4	V	DB17-0, CL1, M, FLM, EQ, DISPTMG, IOL= -400uA
Input Leakage Current	Iil	-	-	±1	uA	IM3-0, CSB, E, R/W, RS, DB17-0, PREGB, VBS, RESETB1, 2, 3
Output Leakage Current	Iol	-	-	±3	uA	DB17-0, CL1, M, FLM, EQ, DISPTMG
Operating Frequency	f_{OSC}	159	177	194	kHz	Target frame frequency = 60 Hz, Display line = 176, Back porch = 3, Front port = 5 Internal RTN[3:0] register = "0000", Internal DIV[1:0] register = "00"

(For the analog circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
LCD Supply Voltage	AVDD	3.5	-	5.5	V	For the analog circuit power
	VGH	9	-	16.5	V	
	VGL	-16.5	-	-9	V	
	Vgoff	-16.5	-	-5.5	V	
	GVDD	3.3	-	5.3	V	
Internal reference power supply voltage	VCI	2.5	-	3.3	V	
Charge-pump for DC-DC regulator	VCI1	1.7	-	3.3	V	1st charge-pump input voltage
	IVCI1	TBD	-	TBD	mA	
	AVDD	TBD	-	-	%	1st charge-pump output efficiency, ILOAD= TBD
	RAVDD	-	TBD	TBD	ohm	
	VCI2	3.4	-	5.5	V	2nd charge-pump input voltage
	VGH	TBD	-	-	%	2nd charge-pump output efficiency, ILOAD= TBD
	RVGH	-	TBD	TBD	kohm	
	VCI3	6.8	-	15	V	3rd charge-pump input voltage
	VGL	TBD	-	-	%	3rd charge-pump output efficiency, ILOAD= TBD
	RVGL	-	TBD	TBD	kohm	
	VCI1 (VCI4)	1.7	-	3.3	V	4th charge-pump input voltage
	VCL	TBD	-	-	%	4th charge-pump output efficiency, ILOAD= TBD
	RVCL	-	TBD	TBD	kohm	
Output Voltage deviation	Vod	-	±20	-	mV	Source Driver
Output Offset between Chips	Voc	-	±20	-	mV	Source Driver
Dynamic Range of Output	Vdr	0.1	-	GVDD-0.1	V	S1 ~ S396
Source Driver Sinking Current of Outputs	ISOL	|-20|	-	-	uA	S1 ~ S396; Vo=1.1V v.s 2.1V AVDD=5V, Gradation output
Source Driver Driving Current of Outputs	ISOH	20	-	-	uA	S1 ~ S396; Vo=4.5V v.s 3.5V AVDD=5V, Gradation output
Gate Driver Sinking Current of Outputs	IGOL	|-250|	-	-	uA	G0 ~ G177; Vo=-12V v.s -11.5V VGH-VGOFF=30V
Gate Driver Driving Current of Outputs	IGOH	250	-	-	uA	G0 ~ G177; Vo=18V v.s 17.5V VGH-VGOFF=30V
Power consumption for Stand-by mode	Isc	-	-	TBD	uA	No load, VDD3=3.3V, VDD=2V, VCI=3.3V, VBS=VSS and all operating is stopped
Operating Current	IVDD	-	TBD	TBD	uA	No load, f_{OSC}=177kHz, VDD3=3.3V, VDD=2V, VCI=3.3V, VBS=VSS, RAM data: 0000h Internal register, NL[4:0] = "10101", RTN[3:0] = "0000", DIV[1:0] = "00" Internal power registers, VC[2:0] = "011", BT[2:0] = "010", VRH[3:0] = "1100", VRL[3:0] = "0110" VCM[4:0] = "10110", VDV[4:0] = "10000", AP[2:0] = "001"
	IVCI	-	TBD	TBD	mA	
Source Driver Output stable time	Tst1	-	TBD	TBD	us	1% or 99% target voltage. CL=30pF, R=4K
Gate Driver Output delay time	Tst2	-	-	TBD	us	10% or 90% target voltage. CL=50pF

(VDD =2.0V, VDD3=3.3V, VSS =0V, TA=25 °C)

(For the regulator circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Reference voltage for internal digital power	RVDD	-	2.0	-	V	VDD3=3.3V
Reference voltage of GVDD	REGP	-	2.5	-	V	VCI=3.3V, VC2-0=”100”
Reference voltage for grayscale voltage generator	GVDD	-	5.83	-	V	VCI=3.3V, VC2-0=”100”, VRH3-0=”1001”
GVDD driving current	IGVDD	TBD	-	-	mA	
Unused pin	GVDD	-	GVDD	-	V	
Low level reference voltage of Vgoff	VGL	-	-6.6	-	V	VCI=3.3V
High level reference voltage of Vcom	VCOMH	-	4.66	-	V	VCI=3.3V, VC2-0=”100”, VRH3-0=”1001”, VCM4-0=”10101”
Low level reference voltage of Vcom	VCOML	-	-1.11	-	V	VCI=3.3V, VC2-0=”100”, VRH3-0=”1001”, VDV4-0=”01101”
VCOM output impedance	RVCMH	-	-	TBD	ohm	ICOM= TBD
	RVCML	-	-	TBD	ohm	ICOM= TBD

(VDD =2.0V, VDD3=3.3V, VSS =0V, TA=25 °C)

(For the PWM circuit)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Base drive current	IDRV	3	-	-	mA	VDD3=3.3V, DRV=0.7V (BJT)
DRV output voltage	VDRV	0	-	VDD3	V	
Feed back voltage	VFB	0.55	0.6	0.65	V	DC/DC operating, VBL current=20mA

(VDD =2.0V, VDD3=3.3V, VSS =0V, TA=25 °C)

AC Electrical Characteristics

(VDD = 2.0V to 2.5V, T_A = -30 to +85 ^oC)

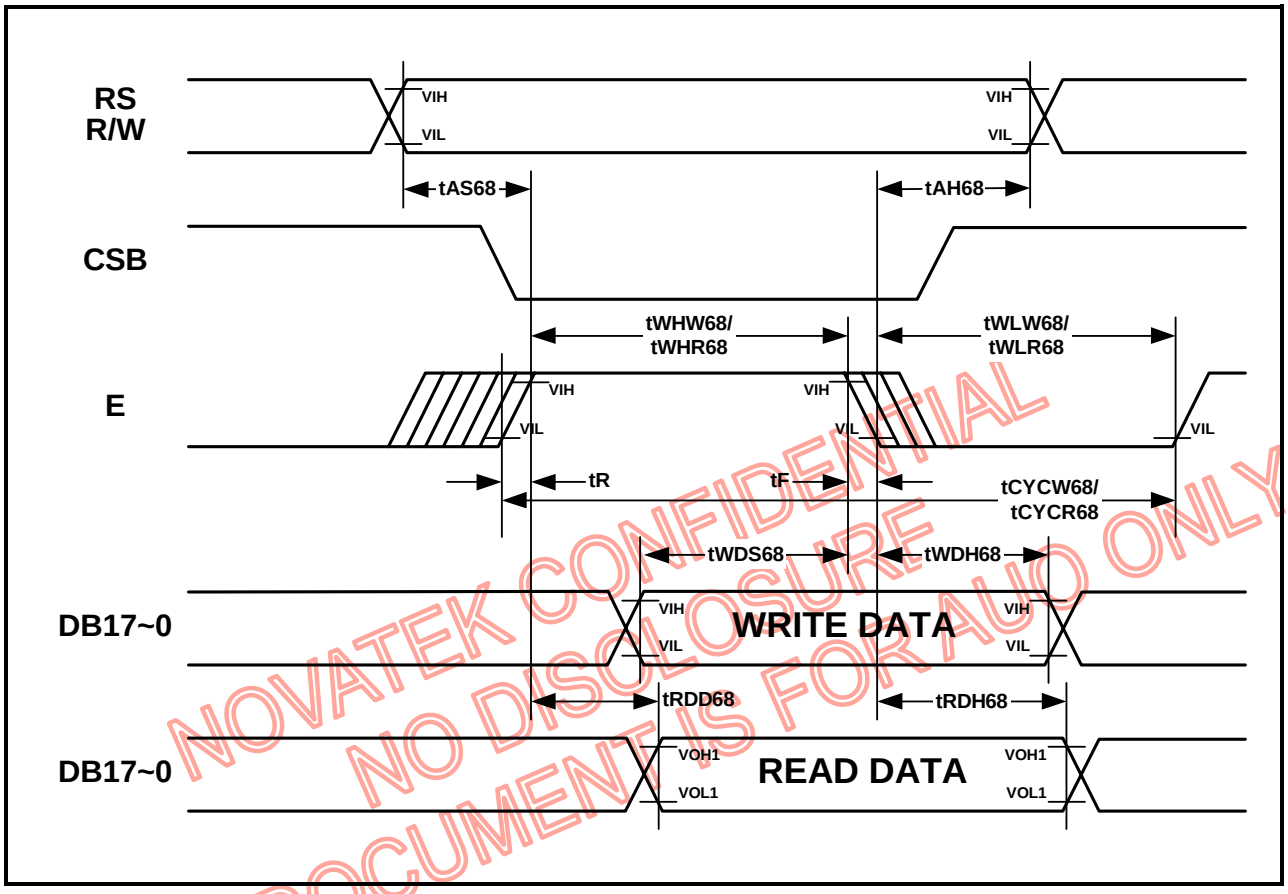
Characteristic		Symbol	VDD3 = 2.5V to 3.3V		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW68}	600	-	ns
	Read	t_{CYCR68}	800		
Pulse rise / fall time		t_R, t_F	-	25	
E pulse width high	Write	t_{WHW68}	90	-	
	Read	t_{WHR68}	350		
E pulse width low	Write	t_{WLW68}	300	-	
	Read	t_{WLR68}	400		
RW, RS and CSB setup time		t_{AS68}	10	-	
RW, RS and CSB hold time		t_{AH68}	5	-	
Write data setup time		t_{WDS68}	60	-	
Write data hold time		t_{WDH68}	15	-	
Read data delay time		t_{RDD68}	-	200	
Read data hold time		t_{RDH68}	5	-	

Table 27. Parallel Write Interface Characteristics (68 Mode, HWM = 0)

(VDD = 2.0V to 2.5V, T_A = -30 to +85 ^oC)

Characteristic		Symbol	VDD3 = 2.5V to 3.3V		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW68}	200	-	ns
	Read	t_{CYCR68}	800		
Pulse rise / fall time		t_R, t_F	-	25	
E pulse width high	Write	t_{WHW68}	90	-	
	Read	t_{WHR68}	350		
E pulse width low	Write	t_{WLW68}	90	-	
	Read	t_{WLR68}	400		
RW, RS and CSB setup time		t_{AS68}	10	-	
RW, RS and CSB hold time		t_{AH68}	5	-	
Write data setup time		t_{WDS68}	60	-	
Write data hold time		t_{WDH68}	15	-	
Read data delay time		t_{RDD68}	-	200	
Read data hold time		t_{RDH68}	5	-	

Table 28. Parallel Write Interface Characteristics (68 Mode, HWM = 1)



AC characteristics (68 Mode, HWM = 0/1)

(VDD = 2.0V to 2.5V, T_A = -30 to +85 ^oC)

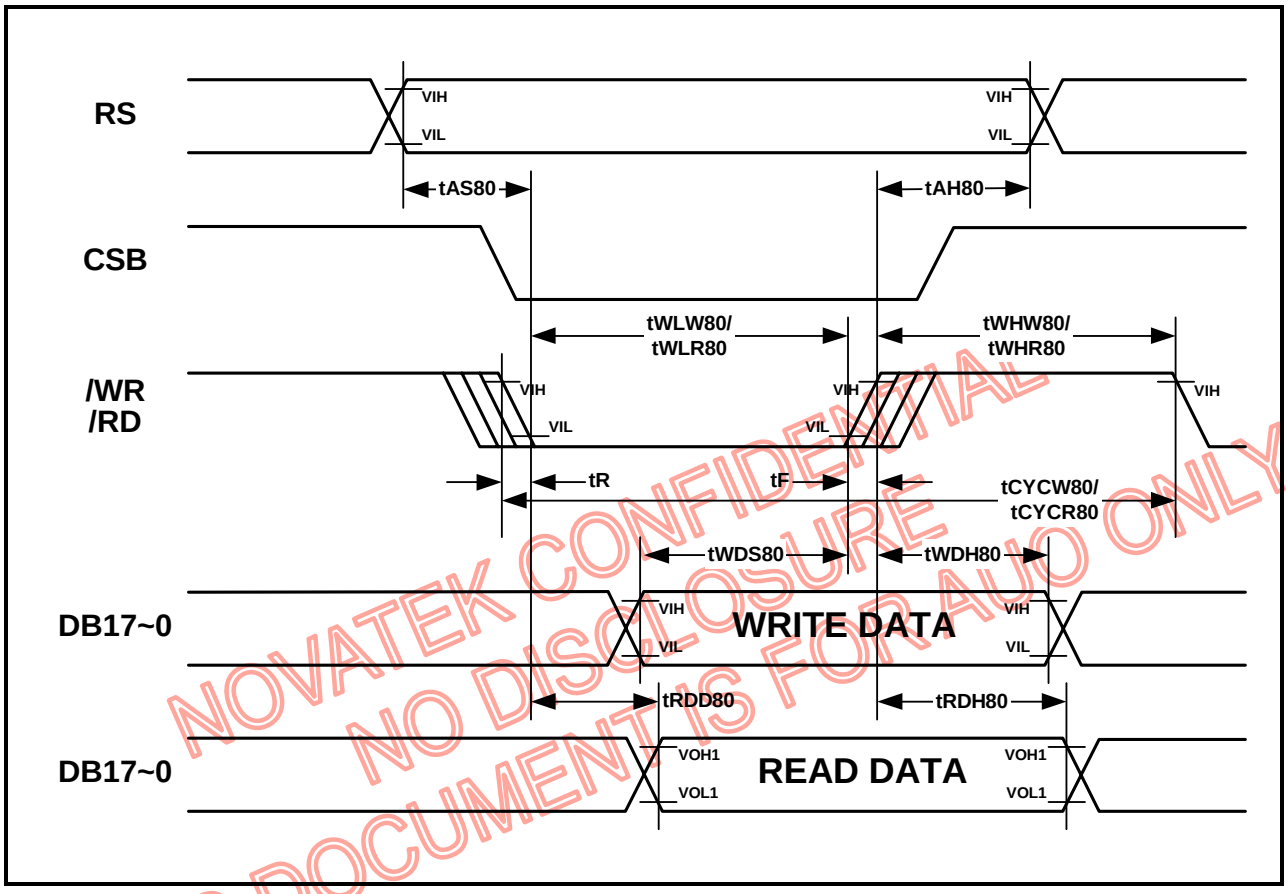
Characteristic		Symbol	VDD3 = 2.5V to 3.3V		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW80}	600	-	ns
	Read	T_{CYCR80}	800		
Pulse rise / fall time		t_R, t_F	-	25	
Pulse width low	Write	T_{WHW80}	90	-	
	Read	T_{WHR80}	350		
Pulse width high	Write	T_{WLW80}	300	-	
	Read	T_{WLR80}	400		
RW, RS and CSB setup time		t_{AS80}	10	-	
RW, RS and CSB hold time		t_{AH80}	5	-	
Write data setup time		t_{WDS80}	60	-	
Write data hold time		t_{WDH80}	15	-	
Read data delay time		t_{RDD80}	-	200	
Read data hold time		t_{RDH80}	5	-	

Table 29. Parallel Write Interface Characteristics (80 Mode, HWM = 0)

(VDD = 2.0V to 2.5V, T_A = -30 to +85 ^oC)

Characteristic		Symbol	VDD3 = 2.5V to 3.3V		Unit
			Min.	Max.	
Cycle time	Write	t_{CYCW80}	200	-	ns
	Read	T_{CYCR80}	800		
Pulse rise / fall time		t_R, t_F	-	25	
Pulse width low	Write	T_{WHW80}	90	-	
	Read	T_{WHR80}	350		
Pulse width high	Write	T_{WLW80}	90	-	
	Read	T_{WLR80}	400		
RW, RS and CSB setup time		t_{AS80}	10	-	
RW, RS and CSB hold time		t_{AH80}	5	-	
Write data setup time		t_{WDS80}	60	-	
Write data hold time		t_{WDH80}	15	-	
Read data delay time		t_{RDD80}	-	200	
Read data hold time		t_{RDH80}	5	-	

Table 30. Parallel Write Interface Characteristics (80 Mode, HWM = 1)



AC characteristics (80 Mode, HWM = 0/1)

(VDD = 2.0V to 2.5V, T_A = -30 to +85 ^oC)

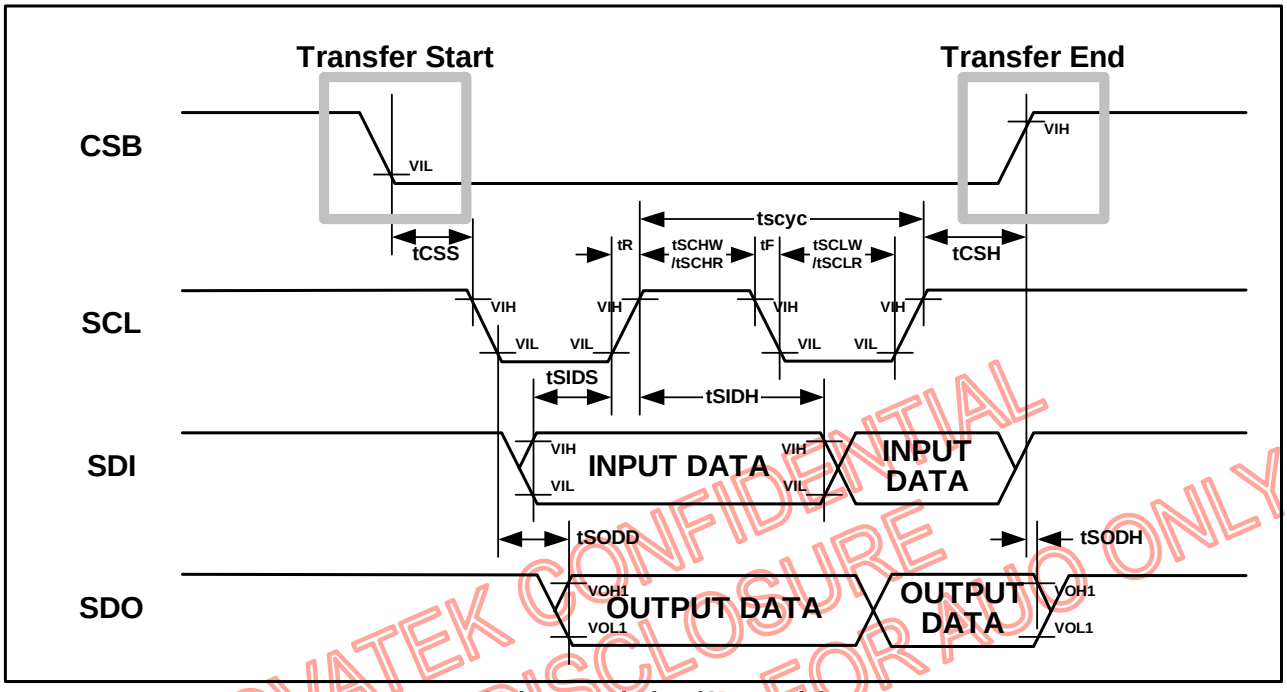
Characteristic	Symbol	VDD3 = 2.5V to 3.3V		Unit
		Min.	Max.	
Serial clock cycle time	tscyc	0.1	20	us
Serial clock rise / fall time	t_R, t_F	-	20	ns
Pulse width high for write	t_{SCHW}	40	-	ns
Pulse width high for read	t_{SCHR}	230	-	ns
Pulse width low for write	t_{SCLW}	60	-	ns
Pulse width low for read	t_{SCLR}	230	-	ns
Chip Select setup time	t_{CSS}	20	-	ns
Chip Select hold time	t_{CSH}	60	-	ns
Serial input data setup time	t_{SIDS}	30	-	ns
Serial input data hold time	t_{SIDH}	30	-	ns
Serial output data delay time	t_{SODD}	-	200	ns
Serial output data hold time	t_{SODH}	5	-	ns

Table 31. Clock Synchronized Serial Write Mode Characteristics

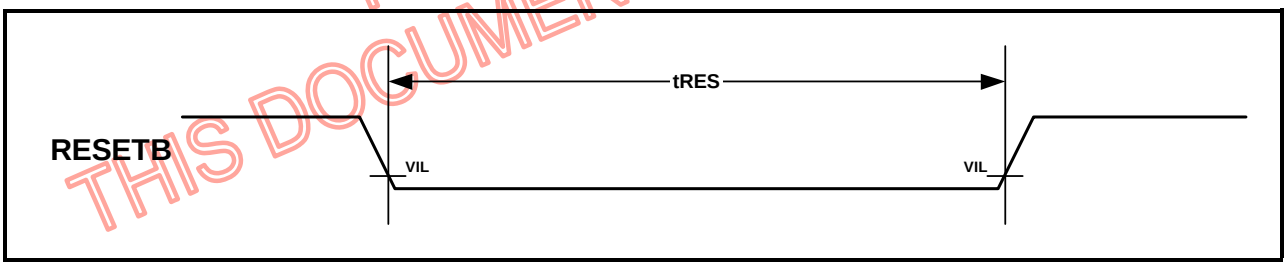
(VDD = 2.0V to 2.5V, T_A = -30 to +85 ^oC)

Characteristic	Symbol	VDD3 = 2.5V to 3.3V		Unit
		Min.	Max.	
Reset low pulse width	t_{RES}	1	-	ms

Table 32. Reset Timing Characteristics



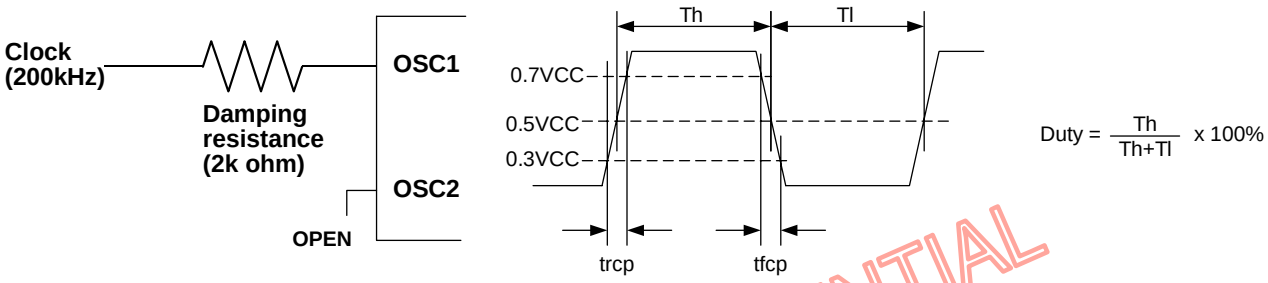
AC characteristics (SPI Mode)



AC characteristics (RESET timing)

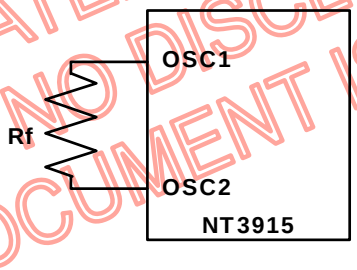
Electrical Characteristics Notes

1. Applies to the external clock input.



External Clock Supply

2. Applies to the internal oscillator operations using external oscillation resistor Rf (figure and table). Shorten these pins' wiring as much as possible, because the number of oscillation wave changes according to the capacity of OSC1, OSC2 pins.



Internal Oscillation

Unit: kHz

Oscillation Resistance (K ohm)	Vcc = 2.5V	Vcc = 3.3V
110 kΩ	T.B.D.	T.B.D.
150 kΩ	T.B.D.	T.B.D.
180 kΩ	T.B.D.	T.B.D.
200 kΩ	T.B.D.	T.B.D.
240 kΩ	T.B.D.	T.B.D.
270 kΩ	T.B.D.	T.B.D.
300 kΩ	T.B.D.	T.B.D.
390 kΩ	T.B.D.	T.B.D.
430 kΩ	T.B.D.	T.B.D.

Table 33. R-C Oscillation Frequency

Bonding Diagram

No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y
1	DUMMY[11]	-8355	-882.76	61	DUMMY[6]	-3400	-882.76	121	DUMMY[6]	1370	-882.76	181	TESTR 2	6022.48	-882.76
2	VCOMOUT_1	-8235	-882.76	62	DB[9]	-3320	-882.76	122	DISPTMG	1450	-882.76	182	VCOMH	6150	-882.76
3	VCOMOUT_1	-8150	-882.76	63	DUMMY[6]	-3240	-882.76	123	VSSO	1535	-882.76	183	VCOMH	6235	-882.76
4	DUMMY	-8065	-882.76	64	DB[8]	-3160	-882.76	124	DUMMY[6]	1615	-882.76	184	VCI1	6320	-882.76
5	C31P	-7980	-882.76	65	DUMMY[6]	-3080	-882.76	125	OSC1	1695	-882.76	185	VCI1	6405	-882.76
6	C31P	-7895	-882.76	66	DB[7]	-3000	-882.76	126	DUMMY[6]	1775	-882.76	186	C41P	6490	-882.76
7	C31M	-7810	-882.76	67	DUMMY[6]	-2920	-882.76	127	OSC2	1855	-882.76	187	C41M	6575	-882.76
8	C31M	-7725	-882.76	68	DB[6]	-2840	-882.76	128	DUMMY[5]	1927.5	-882.76	188	VCL	6660	-882.76
9	VCI3	-7640	-882.76	69	DUMMY[6]	-2760	-882.76	129	DUMMY[5]	1987.5	-882.76	189	REGP	6758.87	-882.76
10	DUMMY[5]	-7567.5	-882.76	70	DB[5]	-2680	-882.76	130	TAVPT	2060	-882.76	190	C11P	6843.87	-882.76
11	VGH	-7495	-882.76	71	DUMMY[6]	-2600	-882.76	131	DUMMY[5]	2132.5	-882.76	191	C11P	6928.87	-882.76
12	VGH	-7410	-882.76	72	DB[4]	-2520	-882.76	132	TAVNT	2205	-882.76	192	C11M	7013.87	-882.76
13	C23P	-7325	-882.76	73	DUMMY[6]	-2440	-882.76	133	DUMMY[5]	2277.5	-882.76	193	C11M	7098.87	-882.76
14	C23P	-7240	-882.76	74	DB[3]	-2360	-882.76	134	TAVO1T	2350	-882.76	194	C12P	7183.87	-882.76
15	C23M	-7155	-882.76	75	DUMMY[6]	-2280	-882.76	135	DUMMY[5]	2422.5	-882.76	195	C12P	7268.87	-882.76
16	C23M	-7070	-882.76	76	DB[2]	-2200	-882.76	136	TESTV2	2495	-882.76	196	C12M	7353.87	-882.76
17	C22P	-6985	-882.76	77	DUMMY[6]	-2120	-882.76	137	VSS	2582.48	-882.76	197	C12M	7438.87	-882.76
18	C22P	-6900	-882.76	78	DB[1]	-2040	-882.76	138	VSS	2667.48	-882.76	198	VGOFF	7523.87	-882.76
19	C22M	-6815	-882.76	79	DUMMY[6]	-1960	-882.76	139	VSS	2752.48	-882.76	199	DUMMY[5]	7604.37	-882.76
20	C22M	-6730	-882.76	80	DB[0]	-1880	-882.76	140	DUMMY[5]	2824.98	-882.76	200	DUMMY[5]	7664.37	-882.76
21	C21P	-6645	-882.76	81	DUMMY[6]	-1800	-882.76	141	DUMMY[5]	2884.98	-882.76	201	FB	7741	-882.76
22	C21P	-6560	-882.76	82	RESETB	-1720	-882.76	142	PREGB	2957.48	-882.76	202	DUMMY[5]	7817.5	-882.76
23	C21M	-6475	-882.76	83	DUMMY[6]	-1640	-882.76	143	VDD3	3042.48	-882.76	203	DRV	7890	-882.76
24	C21M	-6390	-882.76	84	R_W	-1560	-882.76	144	VDD3	3127.48	-882.76	204	DRV	7975	-882.76
25	VCI2	-6305	-882.76	85	DUMMY[6]	-1480	-882.76	145	VDD	3212.48	-882.76	205	DUMMY	8060	-882.76
26	AVDD	-6220	-882.76	86	E	-1400	-882.76	146	VDD	3297.48	-882.76	206	VCOMOUT_2	8145	-882.76
27	AVDD	-6135	-882.76	87	DUMMY[6]	-1320	-882.76	147	RVDD	3382.48	-882.76	207	VCOMOUT_2	8230	-882.76
28	CGND	-6050	-882.76	88	RS	-1240	-882.76	148	RVDD	3467.48	-882.76	208	DUMMY[2]	8355	-882.76
29	CGND	-5965	-882.76	89	DUMMY[6]	-1160	-882.76	149	VCI	3552.48	-882.76	209	DUMMY[3]	8355	922
30	CGND	-5880	-882.76	90	CSB	-1080	-882.76	150	VCI	3637.48	-882.76	210	G[2]	8250	918
31	VGL	-5795	-882.76	91	DUMMY[5]	-1007.5	-882.76	151	VCI	3722.48	-882.76	211	G[4]	8225	805
32	VGL	-5710	-882.76	92	MTEST1	-935	-882.76	152	VBS	3807.48	-882.76	212	G[6]	8200	918
33	VGL	-5625	-882.76	93	DUMMY[6]	-855	-882.76	153	VSSO	3892.48	-882.76	213	G[8]	8175	805
34	AVSS	-5540	-882.76	94	MTEST2	-775	-882.76	154	VGS	3977.48	-882.76	214	G[10]	8150	918
35	AVSS	-5455	-882.76	95	DUMMY[6]	-695	-882.76	155	VGS	4062.48	-882.76	215	G[12]	8125	805
36	AVSS	-5370	-882.76	96	TESTV1	-615	-882.76	156	VCOML	4147.48	-882.76	216	G[14]	8100	918
37	DUMMY[5]	-5297.5	-882.76	97	DUMMY[6]	-535	-882.76	157	VCOML	4232.48	-882.76	217	G[16]	8075	805
38	IM[0]	-5225	-882.76	98	TESTA2	-455	-882.76	158	CGND	4317.48	-882.76	218	G[18]	8050	918
39	DUMMY[5]	-5152.5	-882.76	99	DUMMY[6]	-375	-882.76	159	CGND	4402.48	-882.76	219	G[20]	8025	805
40	IM[1]	-5080	-882.76	100	TESTA3	-295	-882.76	160	GVDD	4487.48	-882.76	220	G[22]	8000	918
41	DUMMY[6]	-5000	-882.76	101	DUMMY[6]	-215	-882.76	161	GVDD	4572.48	-882.76	221	G[24]	7975	805
42	IM[2]	-4920	-882.76	102	TESTA4	-135	-882.76	162	VCOMR	4657.48	-882.76	222	G[26]	7950	918
43	DUMMY[6]	-4840	-882.76	103	DUMMY[6]	-55	-882.76	163	DUMMY[5]	4729.98	-882.76	223	G[28]	7925	805
44	IM[3]	-4760	-882.76	104	TEST	25	-882.76	164	DUMMY[5]	4789.98	-882.76	224	G[30]	7900	918
45	DUMMY[6]	-4680	-882.76	105	DUMMY[6]	105	-882.76	165	TESTB0	4862.48	-882.76	225	G[32]	7875	805
46	DB[17]	-4600	-882.76	106	TS6	185	-882.76	166	DUMMY[5]	4934.98	-882.76	226	G[34]	7850	918
47	DUMMY[6]	-4520	-882.76	107	DUMMY[6]	265	-882.76	167	TESTB1	5007.48	-882.76	227	G[36]	7825	805
48	DB[16]	-4440	-882.76	108	TS7	345	-882.76	168	DUMMY[5]	5079.98	-882.76	228	G[38]	7800	918
49	DUMMY[6]	-4360	-882.76	109	DUMMY[6]	425	-882.76	169	TESTB2	5152.48	-882.76	229	G[40]	7775	805
50	DB[15]	-4280	-882.76	110	VTESTS	505	-882.76	170	DUMMY[5]	5224.98	-882.76	230	G[42]	7750	918
51	DUMMY[6]	-4200	-882.76	111	DUMMY[6]	585	-882.76	171	TESTC0	5297.48	-882.76	231	G[44]	7725	805
52	DB[14]	-4120	-882.76	112	DCTEST	665	-882.76	172	DUMMY[5]	5369.98	-882.76	232	G[46]	7700	918
53	DUMMY[6]	-4040	-882.76	113	DUMMY[5]	737.5	-882.76	173	TESTC1	5442.48	-882.76	233	G[48]	7675	805
54	DB[13]	-3960	-882.76	114	CL1	810	-882.76	174	DUMMY[5]	5514.98	-882.76	234	G[50]	7650	918
55	DUMMY[6]	-3880	-882.76	115	DUMMY[6]	890	-882.76	175	TESTC2	5587.48	-882.76	235	G[52]	7625	805
56	DB[12]	-3800	-882.76	116	M	970	-882.76	176	DUMMY[5]	5659.98	-882.76	236	G[54]	7600	918
57	DUMMY[6]	-3720	-882.76	117	DUMMY[6]	1050	-882.76	177	TESTR0	5732.48	-882.76	237	G[56]	7575	805
58	DB[11]	-3640	-882.76	118	FLM	1130	-882.76	178	DUMMY[5]	5804.98	-882.76	238	G[58]	7550	918
59	DUMMY[6]	-3560	-882.76	119	DUMMY[6]	1210	-882.76	179	TESTR 1	5877.48	-882.76	239	G[60]	7525	805
60	DB[10]	-3480	-882.76	120	EQ	1290	-882.76	180	DUMMY[5]	5949.98	-882.76	240	G[62]	7500	918

No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y
241	G[64]	7475	805	301	VCOMOUT_4	5975	805	361	S[340]	3375	805	421	S[280]	1875	805
242	G[66]	7450	918	302	VCOMOUT_4	5950	918	362	S[339]	3350	918	422	S[279]	1850	918
243	G[68]	7425	805	303	DUMMY	4825	805	363	S[338]	3325	805	423	S[278]	1825	805
244	G[70]	7400	918	304	DUMMY	4800	918	364	S[337]	3300	918	424	S[277]	1800	918
245	G[72]	7375	805	305	S[396]	4775	805	365	S[336]	3275	805	425	S[276]	1775	805
246	G[74]	7350	918	306	S[395]	4750	918	366	S[335]	3250	918	426	S[275]	1750	918
247	G[76]	7325	805	307	S[394]	4725	805	367	S[334]	3225	805	427	S[274]	1725	805
248	G[78]	7300	918	308	S[393]	4700	918	368	S[333]	3200	918	428	S[273]	1700	918
249	G[80]	7275	805	309	S[392]	4675	805	369	S[332]	3175	805	429	S[272]	1675	805
250	G[82]	7250	918	310	S[391]	4650	918	370	S[331]	3150	918	430	S[271]	1650	918
251	G[84]	7225	805	311	S[390]	4625	805	371	S[330]	3125	805	431	S[270]	1625	805
252	G[86]	7200	918	312	S[389]	4600	918	372	S[329]	3100	918	432	S[269]	1600	918
253	G[88]	7175	805	313	S[388]	4575	805	373	S[328]	3075	805	433	S[268]	1575	805
254	G[90]	7150	918	314	S[387]	4550	918	374	S[327]	3050	918	434	S[267]	1550	918
255	G[92]	7125	805	315	S[386]	4525	805	375	S[326]	3025	805	435	S[266]	1525	805
256	G[94]	7100	918	316	S[385]	4500	918	376	S[325]	3000	918	436	S[265]	1500	918
257	G[96]	7075	805	317	S[384]	4475	805	377	S[324]	2975	805	437	S[264]	1475	805
258	G[98]	7050	918	318	S[383]	4450	918	378	S[323]	2950	918	438	S[263]	1450	918
259	G[100]	7025	805	319	S[382]	4425	805	379	S[322]	2925	805	439	S[262]	1425	805
260	G[102]	7000	918	320	S[381]	4400	918	380	S[321]	2900	918	440	S[261]	1400	918
261	G[104]	6975	805	321	S[380]	4375	805	381	S[320]	2875	805	441	S[260]	1375	805
262	G[106]	6950	918	322	S[379]	4350	918	382	S[319]	2850	918	442	S[259]	1350	918
263	G[108]	6925	805	323	S[378]	4325	805	383	S[318]	2825	805	443	S[258]	1325	805
264	G[110]	6900	918	324	S[377]	4300	918	384	S[317]	2800	918	444	S[257]	1300	918
265	G[112]	6875	805	325	S[376]	4275	805	385	S[316]	2775	805	445	S[256]	1275	805
266	G[114]	6850	918	326	S[375]	4250	918	386	S[315]	2750	918	446	S[255]	1250	918
267	G[116]	6825	805	327	S[374]	4225	805	387	S[314]	2725	805	447	S[254]	1225	805
268	G[118]	6800	918	328	S[373]	4200	918	388	S[313]	2700	918	448	S[253]	1200	918
269	G[120]	6775	805	329	S[372]	4175	805	389	S[312]	2675	805	449	S[252]	1175	805
270	G[122]	6750	918	330	S[371]	4150	918	390	S[311]	2650	918	450	S[251]	1150	918
271	G[124]	6725	805	331	S[370]	4125	805	391	S[310]	2625	805	451	S[250]	1125	805
272	G[126]	6700	918	332	S[369]	4100	918	392	S[309]	2600	918	452	S[249]	1100	918
273	G[128]	6675	805	333	S[368]	4075	805	393	S[308]	2575	805	453	S[248]	1075	805
274	G[130]	6650	918	334	S[367]	4050	918	394	S[307]	2550	918	454	S[247]	1050	918
275	G[132]	6625	805	335	S[366]	4025	805	395	S[306]	2525	805	455	S[246]	1025	805
276	G[134]	6600	918	336	S[365]	4000	918	396	S[305]	2500	918	456	S[245]	1000	918
277	G[136]	6575	805	337	S[364]	3975	805	397	S[304]	2475	805	457	S[244]	975	805
278	G[138]	6550	918	338	S[363]	3950	918	398	S[303]	2450	918	458	S[243]	950	918
279	G[140]	6525	805	339	S[362]	3925	805	399	S[302]	2425	805	459	S[242]	925	805
280	G[142]	6500	918	340	S[361]	3900	918	400	S[301]	2400	918	460	S[241]	900	918
281	G[144]	6475	805	341	S[360]	3875	805	401	S[300]	2375	805	461	S[240]	875	805
282	G[146]	6450	918	342	S[359]	3850	918	402	S[299]	2350	918	462	S[239]	850	918
283	G[148]	6425	805	343	S[358]	3825	805	403	S[298]	2325	805	463	S[238]	825	805
284	G[150]	6400	918	344	S[357]	3800	918	404	S[297]	2300	918	464	S[237]	800	918
285	G[152]	6375	805	345	S[356]	3775	805	405	S[296]	2275	805	465	S[236]	775	805
286	G[154]	6350	918	346	S[355]	3750	918	406	S[295]	2250	918	466	S[235]	750	918
287	G[156]	6325	805	347	S[354]	3725	805	407	S[294]	2225	805	467	S[234]	725	805
288	G[158]	6300	918	348	S[353]	3700	918	408	S[293]	2200	918	468	S[233]	700	918
289	G[160]	6275	805	349	S[352]	3675	805	409	S[292]	2175	805	469	S[232]	675	805
290	G[162]	6250	918	350	S[351]	3650	918	410	S[291]	2150	918	470	S[231]	650	918
291	G[164]	6225	805	351	S[350]	3625	805	411	S[290]	2125	805	471	S[230]	625	805
292	G[166]	6200	918	352	S[349]	3600	918	412	S[289]	2100	918	472	S[229]	600	918
293	G[168]	6175	805	353	S[348]	3575	805	413	S[288]	2075	805	473	S[228]	575	805
294	G[170]	6150	918	354	S[347]	3550	918	414	S[287]	2050	918	474	S[227]	550	918
295	G[172]	6125	805	355	S[346]	3525	805	415	S[286]	2025	805	475	S[226]	525	805
296	G[174]	6100	918	356	S[345]	3500	918	416	S[285]	2000	918	476	S[225]	500	918
297	G[176]	6075	805	357	S[344]	3475	805	417	S[284]	1975	805	477	S[224]	475	805
298	G[177]	6050	918	358	S[343]	3450	918	418	S[283]	1950	918	478	S[223]	450	918
299	DUMMY	6025	805	359	S[342]	3425	805	419	S[282]	1925	805	479	S[222]	425	805
300	DUMMY	6000	918	360	S[341]	3400	918	420	S[281]	1900	918	480	S[221]	400	918

No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y
481	S[220]	375	805	541	S[160]	-1125	805	601	S[100]	-2625	805	661	S[40]	-4125	805
482	S[219]	350	918	542	S[159]	-1150	918	602	S[99]	-2650	918	662	S[39]	-4150	918
483	S[218]	325	805	543	S[158]	-1175	805	603	S[98]	-2675	805	663	S[38]	-4175	805
484	S[217]	300	918	544	S[157]	-1200	918	604	S[97]	-2700	918	664	S[37]	-4200	918
485	S[216]	275	805	545	S[156]	-1225	805	605	S[96]	-2725	805	665	S[36]	-4225	805
486	S[215]	250	918	546	S[155]	-1250	918	606	S[95]	-2750	918	666	S[35]	-4250	918
487	S[214]	225	805	547	S[154]	-1275	805	607	S[94]	-2775	805	667	S[34]	-4275	805
488	S[213]	200	918	548	S[153]	-1300	918	608	S[93]	-2800	918	668	S[33]	-4300	918
489	S[212]	175	805	549	S[152]	-1325	805	609	S[92]	-2825	805	669	S[32]	-4325	805
490	S[211]	150	918	550	S[151]	-1350	918	610	S[91]	-2850	918	670	S[31]	-4350	918
491	S[210]	125	805	551	S[150]	-1375	805	611	S[90]	-2875	805	671	S[30]	-4375	805
492	S[209]	100	918	552	S[149]	-1400	918	612	S[89]	-2900	918	672	S[29]	-4400	918
493	S[208]	75	805	553	S[148]	-1425	805	613	S[88]	-2925	805	673	S[28]	-4425	805
494	S[207]	50	918	554	S[147]	-1450	918	614	S[87]	-2950	918	674	S[27]	-4450	918
495	S[206]	25	805	555	S[146]	-1475	805	615	S[86]	-2975	805	675	S[26]	-4475	805
496	S[205]	0	918	556	S[145]	-1500	918	616	S[85]	-3000	918	676	S[25]	-4500	918
497	S[204]	-25	805	557	S[144]	-1525	805	617	S[84]	-3025	805	677	S[24]	-4525	805
498	S[203]	-50	918	558	S[143]	-1550	918	618	S[83]	-3050	918	678	S[23]	-4550	918
499	S[202]	-75	805	559	S[142]	-1575	805	619	S[82]	-3075	805	679	S[22]	-4575	805
500	S[201]	-100	918	560	S[141]	-1600	918	620	S[81]	-3100	918	680	S[21]	-4600	918
501	S[200]	-125	805	561	S[140]	-1625	805	621	S[80]	-3125	805	681	S[20]	-4625	805
502	S[199]	-150	918	562	S[139]	-1650	918	622	S[79]	-3150	918	682	S[19]	-4650	918
503	S[198]	-175	805	563	S[138]	-1675	805	623	S[78]	-3175	805	683	S[18]	-4675	805
504	S[197]	-200	918	564	S[137]	-1700	918	624	S[77]	-3200	918	684	S[17]	-4700	918
505	S[196]	-225	805	565	S[136]	-1725	805	625	S[76]	-3225	805	685	S[16]	-4725	805
506	S[195]	-250	918	566	S[135]	-1750	918	626	S[75]	-3250	918	686	S[15]	-4750	918
507	S[194]	-275	805	567	S[134]	-1775	805	627	S[74]	-3275	805	687	S[14]	-4775	805
508	S[193]	-300	918	568	S[133]	-1800	918	628	S[73]	-3300	918	688	S[13]	-4800	918
509	S[192]	-325	805	569	S[132]	-1825	805	629	S[72]	-3325	805	689	S[12]	-4825	805
510	S[191]	-350	918	570	S[131]	-1850	918	630	S[71]	-3350	918	690	S[11]	-4850	918
511	S[190]	-375	805	571	S[130]	-1875	805	631	S[70]	-3375	805	691	S[10]	-4875	805
512	S[189]	-400	918	572	S[129]	-1900	918	632	S[69]	-3400	918	692	S[9]	-4900	918
513	S[188]	-425	805	573	S[128]	-1925	805	633	S[68]	-3425	805	693	S[8]	-4925	805
514	S[187]	-450	918	574	S[127]	-1950	918	634	S[67]	-3450	918	694	S[7]	-4950	918
515	S[186]	-475	805	575	S[126]	-1975	805	635	S[66]	-3475	805	695	S[6]	-4975	805
516	S[185]	-500	918	576	S[125]	-2000	918	636	S[65]	-3500	918	696	S[5]	-5000	918
517	S[184]	-525	805	577	S[124]	-2025	805	637	S[64]	-3525	805	697	S[4]	-5025	805
518	S[183]	-550	918	578	S[123]	-2050	918	638	S[63]	-3550	918	698	S[3]	-5050	918
519	S[182]	-575	805	579	S[122]	-2075	805	639	S[62]	-3575	805	699	S[2]	-5075	805
520	S[181]	-600	918	580	S[121]	-2100	918	640	S[61]	-3600	918	700	S[1]	-5100	918
521	S[180]	-625	805	581	S[120]	-2125	805	641	S[60]	-3625	805	701	DUMMY	-5125	805
522	S[179]	-650	918	582	S[119]	-2150	918	642	S[59]	-3650	918	702	DUMMY	-5150	918
523	S[178]	-675	805	583	S[118]	-2175	805	643	S[58]	-3675	805	703	VCOMOUT_3	-5950	918
524	S[177]	-700	918	584	S[117]	-2200	918	644	S[57]	-3700	918	704	VCOMOUT_3	-5975	805
525	S[176]	-725	805	585	S[116]	-2225	805	645	S[56]	-3725	805	705	DUMMY	-6000	918
526	S[175]	-750	918	586	S[115]	-2250	918	646	S[55]	-3750	918	706	DUMMY	-6025	805
527	S[174]	-775	805	587	S[114]	-2275	805	647	S[54]	-3775	805	707	G[175]	-6050	918
528	S[173]	-800	918	588	S[113]	-2300	918	648	S[53]	-3800	918	708	G[173]	-6075	805
529	S[172]	-825	805	589	S[112]	-2325	805	649	S[52]	-3825	805	709	G[171]	-6100	918
530	S[171]	-850	918	590	S[111]	-2350	918	650	S[51]	-3850	918	710	G[169]	-6125	805
531	S[170]	-875	805	591	S[110]	-2375	805	651	S[50]	-3875	805	711	G[167]	-6150	918
532	S[169]	-900	918	592	S[109]	-2400	918	652	S[49]	-3900	918	712	G[165]	-6175	805
533	S[168]	-925	805	593	S[108]	-2425	805	653	S[48]	-3925	805	713	G[163]	-6200	918
534	S[167]	-950	918	594	S[107]	-2450	918	654	S[47]	-3950	918	714	G[161]	-6225	805
535	S[166]	-975	805	595	S[106]	-2475	805	655	S[46]	-3975	805	715	G[159]	-6250	918
536	S[165]	-1000	918	596	S[105]	-2500	918	656	S[45]	-4000	918	716	G[157]	-6275	805
537	S[164]	-1025	805	597	S[104]	-2525	805	657	S[44]	-4025	805	717	G[155]	-6300	918
538	S[163]	-1050	918	598	S[103]	-2550	918	658	S[43]	-4050	918	718	G[153]	-6325	805
539	S[162]	-1075	805	599	S[102]	-2575	805	659	S[42]	-4075	805	719	G[151]	-6350	918
540	S[161]	-1100	918	600	S[101]	-2600	918	660	S[41]	-4100	918	720	G[149]	-6375	805

No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y	No	Pad Name	X	Y
721	G[147]	-6400	918	781	G[27]	-7900	918								
722	G[145]	-6425	805	782	G[25]	-7925	805								
723	G[143]	-6450	918	783	G[23]	-7950	918								
724	G[141]	-6475	805	784	G[21]	-7975	805								
725	G[139]	-6500	918	785	G[19]	-8000	918								
726	G[137]	-6525	805	786	G[17]	-8025	805								
727	G[135]	-6550	918	787	G[15]	-8050	918								
728	G[133]	-6575	805	788	G[13]	-8075	805								
729	G[131]	-6600	918	789	G[11]	-8100	918								
730	G[129]	-6625	805	790	G[9]	-8125	805								
731	G[127]	-6650	918	791	G[7]	-8150	918								
732	G[125]	-6675	805	792	G[5]	-8175	805								
733	G[123]	-6700	918	792	G[3]	-8200	918								
734	G[121]	-6725	805	794	G[1]	-8225	805								
735	G[119]	-6750	918	795	G[0]	-8250	918								
736	G[117]	-6775	805	796	DUMMY[4]	-8355	922								
737	G[115]	-6800	918												
738	G[113]	-6825	805												
739	G[111]	-6850	918												
740	G[109]	-6875	805												
741	G[107]	-6900	918												
742	G[105]	-6925	805												
743	G[103]	-6950	918												
744	G[101]	-6975	805												
745	G[99]	-7000	918												
746	G[97]	-7025	805												
747	G[95]	-7050	918												
748	G[93]	-7075	805												
749	G[91]	-7100	918												
750	G[89]	-7125	805												
751	G[87]	-7150	918												
752	G[85]	-7175	805												
753	G[83]	-7200	918												
754	G[81]	-7225	805												
755	G[79]	-7250	918												
756	G[77]	-7275	805												
757	G[75]	-7300	918												
758	G[73]	-7325	805												
759	G[71]	-7350	918												
760	G[69]	-7375	805												
761	G[67]	-7400	918												
762	G[65]	-7425	805												
763	G[63]	-7450	918												
764	G[61]	-7475	805												
765	G[59]	-7500	918												
766	G[57]	-7525	805												
767	G[55]	-7550	918												
768	G[53]	-7575	805												
769	G[51]	-7600	918												
770	G[49]	-7625	805												
771	G[47]	-7650	918												
772	G[45]	-7675	805												
773	G[43]	-7700	918												
774	G[41]	-7725	805												
775	G[39]	-7750	918												
776	G[37]	-7775	805												
777	G[35]	-7800	918												
778	G[33]	-7825	805												
779	G[31]	-7850	918												
780	G[29]	-7875	805												